ATCA-7370/ATCA-7370-S

Installation and Use

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ARTESYN™

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About this Manual

Overview of Contents

This manual is intended for users qualified in electronics or electrical engineering. Users must have a working understanding of Peripheral Component Interconnect (PCI), AdvancedTCA®, and telecommunications.

The manual contains the following chapters and appendices:

- *About this Manual* on page 19 lists all conventions and abbreviations used in this manual and outlines the revision history.
- *Safety Notes* on page 25 lists safety notes applicable to the blade.
- *Sicherheitshinweise* on page 31 provides the German translation of the safety notes section.
- *Introduction* on page 37 describes the main features of the blade.
- *Hardware Preparation and Installation* on page 45 outlines the installation requirements, hardware accessories, switch settings, installation and removal procedures.
- *Controls, Indicators, and Connectors* on page 61 describes external interfaces of the blade. This includes connectors and LEDs.
- *BIOS, on page 75* describes the features and setup of BIOS.
- *Functional Description* on page 103 describes the functional blocks of the blade in detail. This includes a block diagram, description of the main components used and so on.
- *Maps and Registers* on page 113 provides information on the blade's maps and registers.
- *Serial Over LAN* on page 175 provides information on how to establish a serial-over LAN session on your blade.
- *Supported IPMI Commands* on page 181 lists all supported IPMI commands.
- *FRU Information and Sensor Data Records* on page 227 provides information on the blade's FRU information and sensor data.
- *Troubleshooting* on page 247, lists the errors, and describes the reasons and solutions to the problems.
- *Related Documentation* on page 249 provides links to further blade-related documentation.

Abbreviations

This document uses the following abbreviations:

Abbreviation	Definition
ATCA	Advanced Telecom Computing Architecture
BBS	Basic Blade Services
BIOS	Basic Input/Output System
DDR	Dual Data Rate (type of SDRAM)
DDR3	Double Data Rate 3 synchronous dynamic random access memory (SDRAM) is the name of the new DDR memory standard that is being developed as the successor to DDR2 SDRAM
DRAM	Dynamic Random Access Memory
ECC	Error Correction Code
EDAC	Error Detection and Correction
EEPROM	Electrically Erasable Programmable Read Only Memory
EMC	Electro-magnetic Compatibility
ESD	Electro-static Discharge
FRU	Field Replaceable Unit
GPIO	General Purpose Input/Output
I2C	Inter Integrated-Circuit Bus (2-wire serial bus and protocol)
I/O	Input/Output
ICH	I/O Control Hub (also called "South Bridge")
IMC	Integrated Memory Controller
IPMB	Intelligent Platform Management Bus
IPMB-L	The IPMB connecting the carrier IPMC to the AMC module
Intel® QuickPath Interconnect (Intel® QPI)	A cache-coherent, link-based Interconnect specification for Intel processors, chipsets, and I/O bridge components.
IPMC	Intelligent Platform Management Controller
IPMI	Intelligent Platform Management Interface

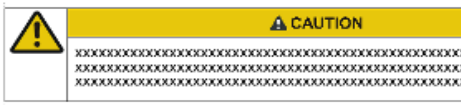
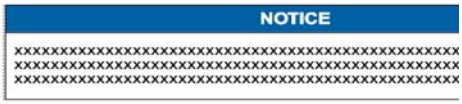
Abbreviation	Definition
JTAG	Joint Test Action Group (test interface for digital logic circuits)
KCS	Keyboard Controller Style
LPC	Low Pin Count
MAC	Medium Access Controller
MMC	Module Management Controller
Module	This term is used to refer to the Module card in this document
MP	Management Power
MTBF	Mean Time Between Failures
NEBS	Network Equipment Building System
NMI	Non-maskable Interrupt
NT	Non-transparent
NVRAM	Non-volatile Random Access Memory
OEM	Original Equipment Manufacturer
PCB	Printed Circuit Board
PCI-E	PCI-Express
PICMG	PCI Industrial Computer Manufacturers Group
PLL	Phase Locked Loop
POST	Power-on Self Test
PP	Payload Power
RTC	Real-Time Clock
Rx	Receive line (of a duplex serial communication interface)
SATA	Serial AT Attachment (high-speed serial interface standard for storage devices)
SCT	SecureCore Tiano
SDR	Sensor Data Record
SDRAM	Synchronous Dynamic Random Access Memory
SELV	Safety Extra Low Voltage
SIMD	Single Instruction Multiple Data

Abbreviation	Definition
SMBus	System Management Bus
SMI	System Management Interrupt
SPD	Serial Presence Detect
Tx	Transmit line (of a duplex serial communication interface)
UART	Universal Asynchronous Receiver-Transmitter

Conventions

The following table describes the conventions used throughout this manual.

Notation	Description
0x00000000	Typical notation for hexadecimal numbers (digits are 0 through F), for example used for addresses and offsets
0b0000	Same for binary numbers (digits are 0 and 1)
bold	Used to emphasize a word
`Screen`	Used for on-screen output and code related elements or commands in body text
`Courier + Bold`	Used to characterize user input and to separate it from system output
Reference	Used for references and for table and figure descriptions
File > Exit	Notation for selecting a submenu
<text>	Notation for variables and keys
[text]	Notation for software buttons to click on the screen and parameter description
...	Repeated item for example node 1, node 2, ..., node 12
. . .	Omission of information from example/command that is not necessary at the time being

Notation	Description
..	Ranges, for example: 0..4 means one of the integers 0,1,2,3, and 4 (used in registers)
|	Logical OR
	Indicates a hazardous situation which, if not avoided, could result in death or serious injury
	Indicates a hazardous situation which, if not avoided, may result in minor or moderate injury
	Indicates a property damage message
	No danger encountered. Pay attention to important information

Summary of Changes

Part Number	Publication Date	Description
6806800P54A	August 2012	Initial Version.
6806800P54B	August 2012	Updated DoC.
6806800P54C	April 2013	This version of the document contains, information about ATCA-7370-Single board variant. Consequently, the title has been updated to reflect this change. Updated Chapter 1, *Introduction, on page 37*, Chapter 2, *Hardware Preparation and Installation, on page 45*, Chapter 5, *Functional Description, on page 103*, Figure 9.1 on page 227.
6806800P54D	August 2013	Updated Chapter 2, *Hardware Preparation and Installation, on page 45*, Table 2-1, and Table 2-2. Added Figure 2-1.
6806800P54E	December 2013	Updated *Safety Notes*.
6806800P54F	June 2014	Re-branded to Artesyn.
6806800P54G	September 2014	Updated the descriptive text in the note for Figure 1-2 on page 42, Figure 2-2 on page 51, Figure 2-3 on page 54, Figure 5-1 on page 103, Figure 5-2 on page 104, Figure 5-4 on page 111, and Figure 9-1 on page 229.

Safety Notes

This section provides warnings that precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed during all phases of operation, service, and repair of this equipment. You should also employ all other safety precautions necessary for the operation of the equipment in your operating environment. Failure to comply with these precautions or with specific warnings elsewhere in this manual could result in personal injury or damage to the equipment.

Artesyn Embedded Technologies intends to provide all necessary information to install and handle the product in this manual. Because of the complexity of this product and its various uses, we do not guarantee that the given information is complete. If you need additional information, ask your Artesyn representative.

The product has been designed to meet the standard industrial safety requirements. It must not be used except in its specific area of office telecommunication industry and industrial control.

Only personnel trained by Artesyn or persons qualified in electronics or electrical engineering are authorized to install, remove or maintain the product.

The information given in this manual is meant to complete the knowledge of a specialist and must not be used as replacement for qualified personnel.

Keep away from live circuits inside the equipment. Operating personnel must not remove equipment covers. Only factory authorized service personnel or other qualified service personnel may remove equipment covers for internal subassembly or component replacement or any internal adjustment.

Do not install substitute parts or perform any unauthorized modification of the equipment or the warranty may be voided. Contact your local Artesyn representative for service and repair to make sure that all safety features are maintained.

EMC

The blade has been tested in a standard Artesyn system and found to comply with the limits for a Class A digital device in this system, pursuant to part 15 of the FCC Rules, EN 55022 Class A respectively. These limits are designed to provide reasonable protection against harmful interference when the system is operated in a commercial environment.

This is a Class A product based on the standard of the Voluntary Control Council for Interference by Information Technology Interference (VCCI). If this equipment is used in a domestic environment, radio disturbance may arise. When such trouble occurs, the user may be required to take corrective actions.

The blade generates and uses radio frequency energy and, if not installed properly and used in accordance with this guide, may cause harmful interference to radio communications. Operating the system in a residential area is likely to cause harmful interference, in which case the user will be required to correct the interference at his own expense.

The USB1, USB2 ports and the COM port are considered as debug/maintenance ports. During normal operation no cables must be connected to these ports. Cables attached to these ports during maintenance must not exceed a length of 3m.

Installation

Damage of Circuits
Electrostatic discharge and incorrect blade installation and removal can damage circuits or shorten their life.
Before touching the blade or electronic components, make sure that you are working in an ESD-safe environment.

Data Loss
Removing the blade with the blue LED still blinking causes data loss.
Wait until the blue LED is permanently illuminated, before removing the blade.

Damage of Blade and Additional Devices and Modules
Incorrect installation of additional devices or modules may damage the blade or the additional devices or modules.
Before installing or removing an additional device or module, read the respective documentation

Operation

Blade Damage
Blade surface
High humidity and condensation on the blade surface causes short circuits.
Do not operate the blade outside the specified environmental limits. Make sure the blade is completely dry and there is no moisture on any surface before applying power.

Blade Overheating and Blade Damage
Operating the blade without forced air cooling may lead to blade overheating and thus blade damage.
When operating the blade, make sure that forced air cooling is available in the shelf.

When operating the blade in areas of electromagnetic radiation ensure that the blade is bolted on the system and the system is shielded by enclosure.

Injuries or Short Circuits
Blade or power supply
In case the ORing diodes of the blade fail, the blade may trigger a short circuit between input line A and input line B so that line A remains powered even if it is disconnected from the power supply circuit (and vice versa).
To avoid damage or injuries, always check that there is no more voltage on the line that has been disconnected before continuing your work.

SFP / SFP+ Modules

Personal Injury and Damage of the RTM and SFP Modules
Installing and using SFP modules which are not fully certified and which do not meet all relevant safety standards may damage the RTM and the SFP modules and may lead to personal injury.
Only use and install SFP modules which are fully certified and which meet all relevant safety standards.

Personal Injury
Optical SFP modules may be classified as laser products. When installing and using any of these SFP modules, the regulations which correspond to the respective laser class apply to the whole RTM. Not complying to these regulations may lead to personal injury.
When installing and using optical SFP modules which are classified as laser products, make sure to comply to the respective regulations.

Eye Damage
Optical SFP modules may emit laser radiation when no cable is connected. This laser radiation is harmful to your eyes.
Do not look into the optical lens at any time.

SFP Module Damage
The optical port plug protects the optical fibres against dirt and damage. Dirt and damage can render the SFP module inoperable.
Only remove the optical plug when you are ready to connect a cable to the SFP module. When no cable is connected, cover the port with an optical port plug.

RJ-45 Connectors

The RJ-45 connectors on the face plate must only be used for twisted-pair Ethernet (TPE) and serial console connections (according to face plate marking). TPE and serial connections are considered SELV circuits. Connecting a telephone line (TNV circuit) to such a connector may destroy your telephone as well as your board. Therefore,

- Clearly mark TPE connectors near your working area as network connectors.
- Only connect TPE bushing of the system to safety extra low voltage (SELV) circuits.
- Make sure that the length of the electric cable connected to a TPE bushing does not exceed 100 m.

If you have further questions, ask your system administrator.

Switch Settings

Blade Malfunction
Switches marked as 'reserved' might carry production-related functions and can cause the blade to malfunction if their setting is changed.
Therefore, do not change settings of switches marked as 'reserved'. The setting of switches which are not marked as 'reserved' has to be checked and changed before blade installation.

Blade Damage
Setting/resetting the switches during operation can cause blade damage.
Therefore, check and change switch settings before you install the blade.

Battery

Blade Damage
Wrong battery installation may result in hazardous explosion and blade damage.
Therefore, always use the same type of Lithium battery as is installed and make sure the battery is installed as described in this manual.

Environment

Always dispose of used blades, system components and RTMs according to your country's legislation and manufacturer's instructions.

Sicherheitshinweise

Dieses Kapitel enthält Hinweise, die potentiell gefährlichen Prozeduren innerhalb dieses Handbuchs vorrangestellt sind. Beachten Sie unbedingt in allen Phasen des Betriebs, der Wartung und der Reparatur des Systems die Anweisungen, die in diesen Hinweisen enthalten sind. Sie sollten außerdem alle anderen Vorsichtsmaßnahmen treffen, die für den Betrieb des Produktes innerhalb Ihrer Betriebsumgebung notwendig sind. Wenn Sie diese Vorsichtsmaßnahmen oder Sicherheitshinweise, die an anderer Stelle diese Handbuchs enthalten sind, nicht beachten, kann das Verletzungen oder Schäden am Produkt zur Folge haben.

Artesyn Embedded Technologies ist darauf bedacht, alle notwendigen Informationen zum Einbau und zum Umgang mit dem Produkt in diesem Handbuch bereit zu stellen. Da es sich jedoch um ein komplexes Produkt mit vielfältigen Einsatzmöglichkeiten handelt, können wir die Vollständigkeit der im Handbuch enthaltenen Informationen nicht garantieren. Falls Sie weitere Informationen benötigen sollten, wenden Sie sich bitte an die für Sie zuständige Geschäftsstelle von Artesyn.

Das System erfüllt die für die Industrie geforderten Sicherheitsvorschriften und darf ausschließlich für Anwendungen in der Telekommunikationsindustrie und im Zusammenhang mit Industriesteuerungen verwendet werden.

Einbau, Wartung und Betrieb dürfen nur von durch Artesyn ausgebildetem oder im Bereich Elektronik oder Elektrotechnik qualifiziertem Personal durchgeführt werden. Die in diesem Handbuch enthaltenen Informationen dienen ausschließlich dazu, das Wissen von Fachpersonal zu ergänzen, können dieses jedoch nicht ersetzen.

Halten Sie sich von stromführenden Leitungen innerhalb des Produktes fern. Entfernen Sie auf keinen Fall Abdeckungen am Produkt. Nur werksseitig zugelassenes Wartungspersonal oder anderweitig qualifiziertes Wartungspersonal darf Abdeckungen entfernen, um Komponenten zu ersetzen oder andere Anpassungen vorzunehmen.

Installieren Sie keine Ersatzteile oder führen Sie keine unerlaubten Veränderungen am Produkt durch, sonst verfällt die Garantie. Wenden Sie sich für Wartung oder Reparatur bitte an die für Sie zuständige Geschäftsstelle von Artesyn. So stellen Sie sicher, dass alle sicherheitsrelevanten Aspekte beachtet werden.

EMV

Das Blade wurde in einem Artesyn Standardsystem getestet. Es erfüllt die für digitale Geräte der Klasse A gültigen Grenzwerte in einem solchen System gemäß den FCC-Richtlinien Abschnitt 15 bzw. EN 55022 Klasse A. Diese Grenzwerte sollen einen angemessenen Schutz vor Störstrahlung beim Betrieb des Blades in Gewerbe- sowie Industriegebieten gewährleisten.

Das Blade arbeitet im Hochfrequenzbereich und erzeugt Störstrahlung. Bei unsachgemäßem Einbau und anderem als in diesem Handbuch beschriebenen Betrieb können Störungen im Hochfrequenzbereich auftreten.

Warnung! Dies ist eine Einrichtung der Klasse A. Diese Einrichtung kann im Wohnbereich Funkstörungen verursachen. In diesem Fall kann vom Betreiber verlangt werden, angemessene Maßnahmen durchzuführen.

Die nachfolgend aufgeführten Schnittstellen sind Wartungsschnittstellen:

USB1, USB2 und COM

Während des Normalbetriebs darf an diesen Schnittstellen kein Kabel angeschlossen sein. Im Wartungsfall angeschlossene Kabel dürfen eine Länge von 3m nicht überschreiten.

Installation

Beschädigung von Schaltkreisen
Elektrostatische Entladung und unsachgemäßer Ein- und Ausbau von Blades kann Schaltkreise beschädigen oder ihre Lebensdauer verkürzen.
Bevor Sie Blades oder elektronische Komponenten berühren, vergewissern Sie sich, daß Sie in einem ESD-geschützten Bereich arbeiten.

Datenverlust
Wenn Sie das Blade aus dem Shelf herausziehen, und die blaue LED blinkt noch, gehen Daten verloren.
Warten Sie bis die blaue LED durchgehend leuchtet, bevor Sie das Blade herausziehen.

Beschädigung des Blades und von Zusatzmodulen
Fehlerhafte Installation von Zusatzmodulen, kann zur Beschädigung des Blades und der Zusatzmodule führen.
Lesen Sie daher vor der Installation von Zusatzmodulen die zugehörige Dokumentation.

RJ-45 Stecker

Die RJ-45 Stecker auf der Frontblende dürfen nur für Twisted-Pair-Ethernet (TPE) oder für Serielle Konsole Verbindungen verwendet werden (entsprechend der Markierung an der Frontblende). TPE und Serielle Verbindungen sind SELV Kreise. Beachten Sie, dass ein versehentliches Anschließen einer Telefonleitung (TNV Kreis) an einen solchen TPE Stecker sowohl das Telefon als auch das Board zerstören kann. Beachten Sie deshalb die folgenden Hinweise:

- Kennzeichnen Sie TPE-Anschlüsse in der Nähe Ihres Arbeitsplatzes deutlich als Netzwerkanschlüsse.
- Schließen Sie an TPE-Buchsen ausschließlich SELV-Kreise (Sicherheitskleinspannungsstromkreise) an.
- Die Länge des mit dem Board verbundenen Twisted-Pair Ethernet-Kabels darf 100 m nicht überschreiten.

Betrieb

Beschädigung des Blades
Hohe Luftfeuchtigkeit und Kondensat auf der Oberfläche des Blades können zu Kurzschlüssen führen.
Betreiben Sie das Blade nur innerhalb der angegebenen Grenzwerte für die relative Luftfeuchtigkeit und Temperatur. Stellen Sie vor dem Einschalten des Stroms sicher, dass sich auf dem Blade kein Kondensat befindet.

Überhitzung und Beschädigung des Blades
Betreiben Sie das Blade ohne Zwangsbelüftung, kann das Blade überhitzt und schließlich beschädigt werden.
Bevor Sie das Blade betreiben, müssen Sie sicher stellen, dass das Shelf über eine Zwangskühlung verfügt.

Wenn Sie das Blade in Gebieten mit starker elektromagnetischer Strahlung betreiben, stellen Sie sicher, dass das Blade mit dem System verschraubt ist und das System durch ein Gehäuse abgeschirmt wird.

Verletzungen oder Kurzschlüsse
Blade oder Stromversorgung
Falls die ORing Dioden des Blades durchbrennen, kann das Blade einen Kurzschluss zwischen den Eingangsleitungen A und B verursachen. In diesem Fall ist Leitung A immer noch unter Spannung, auch wenn sie vom Versorgungskreislauf getrennt ist (und umgekehrt).
Prüfen Sie deshalb immer, ob die Leitung spannungsfrei ist, bevor Sie Ihre Arbeit fortsetzen, um Schäden oder Verletzungen zu vermeiden.

SFP / SFP+ Modules

Gefahr von Verletzungen sowie von Beschädigung des RTMs und SFP-Modulen
Die Installation und der Betrieb von SFP-Modulen, welche nicht zertifiziert sind und welche nicht den Sicherheitsstandards entsprechen, kann Verletzungen zur Folge haben sowie zur Beschädigung des RTMs und von SFP-Modulen führen.
Verwenden Sie daher nur SFP-Module, die zertifiziert sind und die den Sicherheitsstandards entsprechen.

Verletzungsgefahr
Optische SFP-Module können als Laserprodukte klassifiziert sein. Wenn Sie solche SFP-Module installieren und betreiben, so gelten die entsprechenden Bestimmungen für Laserprodukte für das gesamte RTM. Werden diese Bestimmungen nicht eingehalten, so können Verletzungen die Folge sein.
Wenn Sie SFP-Module betreiben, die als Laserprodukte klassifiziert sind, stellen Sie sicher, dass die entsprechenden Bestimmungen für Laserprodukte eingehalten werden.

Verletzungsgefahr der Augen
Optische SFP-Module können Laserstrahlen aussenden, wenn kein Kabel angeschlossen ist. Blicken Sie daher nicht direkt in die Öffnung eines SFP-Moduls, um Verletzungen der Augen zu vermeiden.

Beschädigung von SFP-Modulen
Die Schutzkappe eines SFP-Modules dient dazu, die sensible Optik des SFP-Modules gegen Staub und Schmutz zu schützen.
Entfernen Sie die Schutzkappe nur dann, wenn Sie beabsichtigen, ein Kabel anzuschließen. Andernfalls belassen Sie die Schutzkappe auf dem SFP-Modul.

Schaltereinstellungen

Fehlfunktion des Blades
Schalter, die mit 'Reserved' gekennzeichnet sind, können mit produktionsrelevanten Funktionen belegt sein. Das Ändern dieser Schalter kann im normalen Betrieb Störungen auslösen.
Verstellen Sie nur solche Schalter, die nicht mit 'Reserved' gekennzeichnet sind. Prüfen und ändern Sie die Einstellungen der nicht mit 'Reserved' gekennzeichneten Schalter, bevor Sie das Blade installieren.

Beschädigung der Blade
Das Verstellen von Schaltern während des laufenden Betriebes kann zur Beschädigung des Blades führen.
Prüfen und ändern Sie die Schaltereinstellungen, bevor Sie das Blade installieren.

Batterie

Beschädigung des Blades
Ein unsachgemäßer Einbau der Batterie kann gefährliche Explosionen und Beschädigungen des Blades zur Folge haben.
Verwenden Sie deshalb nur den Batterietyp, der auch bereits eingesetzt wurde und befolgen Sie die Installationsanleitung.

Umweltschutz

Entsorgen Sie alte Batterien und/oder Blades/Systemkomponenten/RTMs stets gemäß der in Ihrem Land gültigen Gesetzgebung und den Empfehlungen des Herstellers.

1.1 Features

The ATCA-7370 is a high performance dual processor AdvancedTCA Server blade and AdvancedTCA Node board, designed according to PICMG 3.0 Revision 3.0 Advanced TCA Base Specification. ATCA-7370 is a single board computer that offers a complex powerful processing through a dual eight-core Intel Xeon E5-2648L processor, and support for up to 128 GByte DDR3 memory and a single processor version.

Furthermore ATCA-7370 provides local storage, standard I/O and redundant Ethernet connections to the back plane's Base Interfaces (PICMG3.0) and Fabric Interfaces (PICMG 3.1 Option1,9). Another important feature is that ATCA-7370 provides system management capabilities and is hot swap compatible based on the ATCA specification.

A single processor variant of the ATCA-7370 is also available. It is called ATCA-7370-S.

The following are the main features of ATCA-7370:

- Form factor: Single slot ATCA (280mm x 322mm)
- Processor: Intel Xeon E5-2648L eight core processor
- PCH (chipset):C604 chipset
- Memory: Total of eight DDR3 DIMM slots, supports up to 128 GB memory with speed rate up to DDR3-1600 and 4 slots in case of single processor variant.
- Base interface: Dual 10/100/1000Base-T Ethernet
- Fabric Interface: Dual 1G/10Gbps Ethernet interfaces, support PICMG3.1 option 1 and 9
- Cave Creek Mezzanine card for compression/decompression or security (optional)
- Front Panel
  - One RJ45 GE Ethernet Port, the other RJ45 GE port (the lower one) is reserved.
  - Two USB2.0 Ports
  - One serial console
  - Reset button
- Onboard IPMI management controller (IPMC) implements IPMI version 1.5
- Onboard Glue Logic FPGA for IPMC extension and onboard Control register

- RTM Interface
  - Total 36 PCI-E Lanes on three Zone3 connectors.
  - 4x SAS port
  - 1x USB interfaces
  - IPMI Management bus
- BIOS Chip: Up to 8MB onboard Boot and 8 MB Recovery Boot Flash (SPI)

1.2 Standard Compliances

The product is designed to meet the following standards.

Table 1-1 Standard Compliances

Standard	Description
SN29500/8	Reliability requirements
MIL-HDBK-217F	
SR-332	
TR-NWT-000357	
IEC 60068-2-1/2/3/13/14	Climatic environmental requirements. The product can only be used in a restricted temperature range.
IEC 60068-2-27/32/35	Mechanical environmental requirements
IEC 60950-1, EN 60950-1, UL/CSA 60950-1	Safety requirements
UL 94V-0/1, Oxygen index for PCBs below 28%	Flammability

Table 1-1 Standard Compliances (continued)

Standard	Description
EN 55022	EMC requirements on system level Attention: ATCA boards require CISPR 22 Class A on conducted emissions EMC immunity requirements industrial EMC for telecom equipment
EN 55024	
EN 300 386 (v1.4.1): 2008	
FCC Part 15, Subpart B	
ICES-003: 2004	
VCCI V-3/2011.04	
AS/NZS CISPR22: 2009	
ANSI/IPC-A-610 Rev.B Class 2	Manufacturing requirements
ANSI/IPC-R-700B, ANSI-J-001...003	
ISO 8601	Y2K compliance
NEBS Standard GR-63-CORE	NEBS level three
NEBS Standard GR-1089 CORE	Project is designed to support NEBS level three. The compliance tests must be done with the customer target system.

Figure 1-1 Declaration of Conformity

Declaration of Conformity (DoC)

According to EN 17050-1:2004

Manufacturer's Name: Artesyn Embedded Technologies

Manufacturer's Address: Artesyn Embedded Technologies GmbH
Lilienthalstrasse 17-19
85579 Neubiberg
Germany

Declares that the following product

Product: **ATCA Blade with Rear Transition Modules**

Model Names / Numbers: **ATCA-7370, ATCA-7370-Cxx, ATCA-7370-S, ATCA-7370-S-Cxx, RTM-ATCA-737X, RTM-ATCA-737X-Cxx**
"x" in model name can be "0" to "9" and defines configuration

in accordance with the requirements of 2004/108/EC, 2006/95/EC & 2011/65/EU and their amending directives, has been designed and manufactured to the following specifications:

EN 60950-1:2006+A12:2011

EN 55022:2010 (Class A)

EN 55024:2010

ETSI EN 300 386 V1.6.1 (2012-09)

2011/65EU RoHS Directive

Kai Holz
Director Engineering

Issue Date: 12/May/2014

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1.3 Mechanical Data

The following table provides details about the blade's mechanical data, such as dimensions and weight.

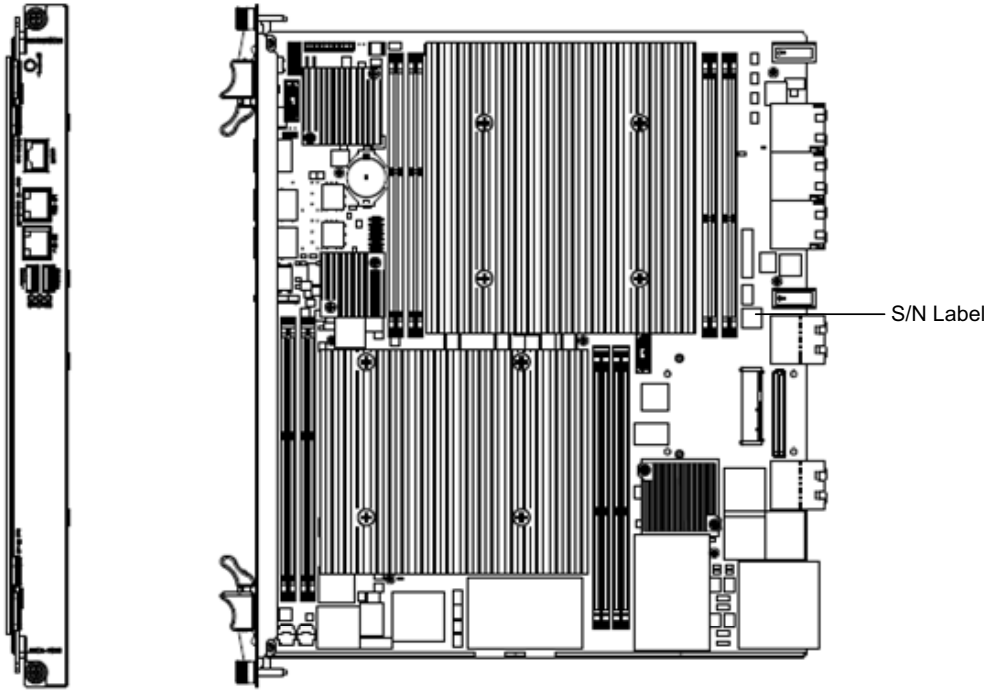
Table 1-2 Mechanical Data

Feature	Value
Dimensions (width x height x depth)	Single slot ATCA 30mm x 351mm x 312mm, 8U form factor
Net weight	2930g (without DIMMs), 2496g (with 4x 8GB DIMMs)
Weight (including Artesyn standard packaging)	4105 g (without DIMMs), 4318 g (with 8x 8GB DIMMs)

1.4 Mechanical Layout

The following graphics illustrate the mechanical layout of the blade.

Figure 1-2 Mechanical Layout



Note: On the single processor variant the processor and its DIMM sockets are populated on the upper side of the board. Components associated with the second processor are not populated on this product variant.

1.5 Mean Time Between Failures

The following table specifies the Mean Time Between Failures (MTBF) data.

ATCA-7370 blade	5470 fit (182,815 hours)
RTM-7370 blade	950 fit (1,052,631 hours)
Standard for calculation	SR332

The following table specifies the environmental conditions required for the blade.

Quality Level	Quality Level II is most common
Environment	Typically Ground, Fixed, Controlled
Assembly Ambient Temperature	40 °C
Confidence Level	60 %

1.6 Ordering Information

As of the printing date of this manual, this guide supports the models listed below.

Table 1-3 Blade Variants - Ordering Information

Product Name	Description
ATCA-7370	ATCA BLADE, DUAL INTEL XEON E5-2600 SERIES 8-CORE PROCESSOR, 0GB, 10G SUPPORT, NSN VARIANT.
ATCA-7370-0GB-S	Single Board Variant.

As of the printing date of this manual, the following board accessories are available.

Table 1-4 Blade Accessories - Ordering Information

Accessory	Description
RTM-ATCA-737x	RTM for the ATCA-737x product series, 2X GBE (SFP), 2X slot for optional HDD, NSN variant.

Table 1-4 Blade Accessories - Ordering Information (continued)

Accessory	Description
ATCA-7370-ACCEL-MOD	Single coprocessor module to accelerate cryptography, data compression, and pattern matching.

1.7 Product Identification

The Figure 1-2 on page 42 shows the location of the serial number label.

2.1 Unpacking and Inspecting the Blade

This section describes the procedure for packing and inspecting the blade.

NOTICE

Damage of Circuits
Electrostatic discharge and incorrect blade installation and removal can damage circuits or shorten its life.
Before touching the blade or electronic components, make sure that you are working in an ESD-safe environment.

Shipment Inspection

To inspect the shipment, perform the following steps.

1. Verify that you have received all items of your shipment:
   - Printed *Quick Start Guide* and *Safety Notes Summary*
   - ATCA-7370 blade
   - Any optional items ordered
2. Check for damage and report any damage or differences to the customer service.
3. Remove the desiccant bag shipped together with the blade and dispose of it according to your country's legislation.

The blade is thoroughly inspected before shipment. If any damage occurred during transportation or any items are missing, please contact our customer service immediately.

2.2 Environmental and Power Requirements

In order to meet the environmental requirements, the blade has to be tested in the system in which it is to be installed.

Before you power up the blade, calculate the power needed according to your combination of blade upgrades and accessories.

2.2.1 Environmental Requirements

The environmental conditions must be tested and proven in the shelf configuration used. The conditions refer to the surrounding of the blade within the user environment.

Table 2-1 Environmental Requirements

Requirement	Operating	Non-Operating
Temperature	+5 °C (41 °F) to +40 °C (104 °F) (normal operation) according to NEBS Standard GR-63-CORE -5 °C (23 °F) to +55 °C (131 °F) (exceptional operation) according to NEBS Standard GR-63-CORE	-40 °C (-40 °F) to +70 °C (158 °F) (may be further limited by installed accessories)
Temp. Change	+/- 0.25 °C/min according to NEBS Standard GR-63-CORE	+/- 0.25 °C/min
Rel. Humidity	5% to 90% non-condensing according to Artesyn-internal environmental requirements	5% to 95% non-condensing according to Artesyn-internal environmental requirements
Vibration	0.1 g from 5 to 100 Hz and back to 5 Hz at a rate of 0.1 octave/minute	5-20 Hz at 0.01 g^2/Hz 20-200 Hz at -3.0 dB/octave Random 5-20 Hz at 1 m^2/Sec^3 Random 20-200 Hz at -3 m/Sec^2
Shock	Half-sine, 11 m/Sec, 30mSec/Sec^2	Blade level packaging Half-sine, 6 mSec at 180 m/Sec^2
Free Fall	-	1,200 mm/all edges and corners 1.0 m (packaged) per ETSI 300 019-2-2 (blade level packaging) 100 mm (unpacked) per GR-63-CORE

- The environmental requirements of the blade may be further limited down due to installed accessories, such as hard disks with more restrictive environmental requirements.
- Operating temperatures refer to the temperature of the air circulating around the blade and not to the actual component temperature.

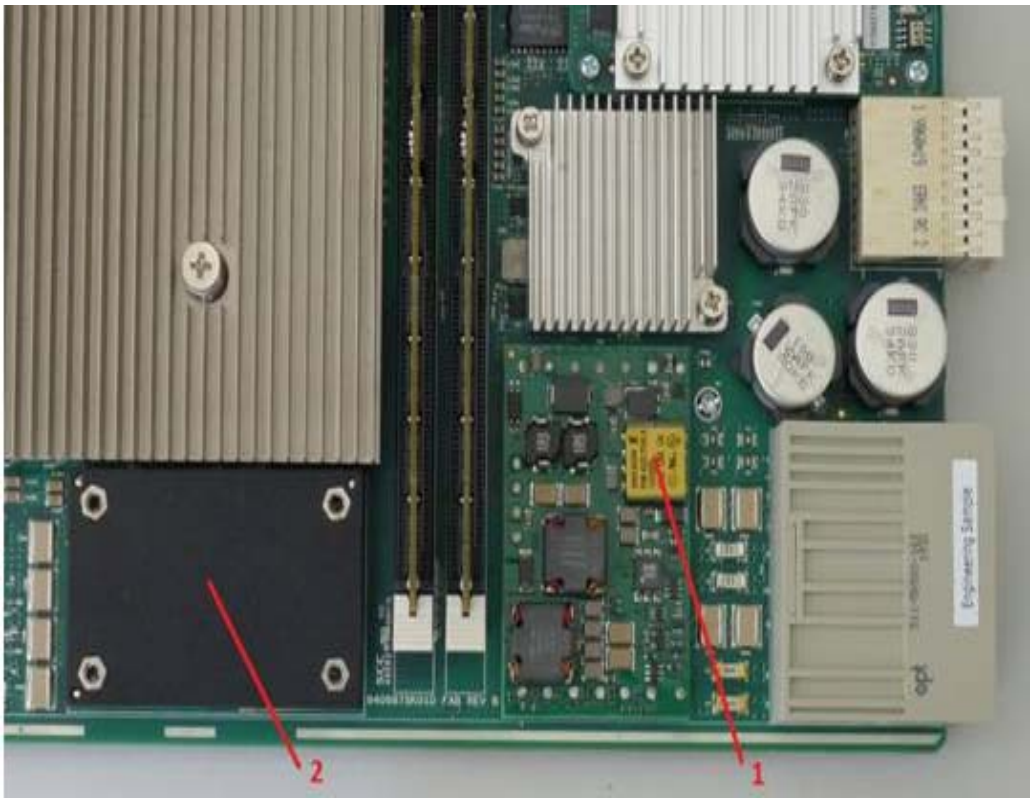
NOTICE

Blade Surface and Blade Damage

High humidity and condensation on the blade surface causes short circuits.
Do not operate the blade outside the specified environmental limits. Make sure the blade is completely dry and there is no moisture on any surface before applying power.

Blade Overheating and Blade Damage
Operating the blade without forced air cooling may lead to blade overheating and thus blade damage.
When operating the blade, make sure that forced air cooling is available on the shelf.

Figure 2-1 Location of Critical Temperature Spots (Blade Top Side)



1. Temperature Spot 1 (on Power Entry Module) Max: 90°C (exact location: on top of the transformer)

2. Temperature Spot 2 (on 48V/12V DC/DC Module): Max: 100°C (exact location: in the geometric middle of the heat spreader)

2.2.2 Power Requirements

The blade's power requirements depend on the installed hardware accessories. If you want to install accessories on the blade, the load of the respective accessory has to be added to that of the blade. For information on the accessories' power requirements, refer to the documentation delivered together with the respective accessory or consult your local Artesyn Embedded Technologies representative for further details.

The blade must be connected to a TNV-2 or a safety-extra-low-voltage (SELV) circuit. A TNV-2 circuit is a circuit whose normal operating voltages exceed the limits for a SELV circuit under normal operating conditions, and which is not subject to over voltages from telecommunication networks.

Table 2-2 Power Requirements

Characteristic	Value
Rated Voltage Exception in the US and Canada	-48 VDC to -60 VDC -48 VDC
Operating Voltage Exception in the US and Canada	-39 VDC to -72 VDC -39 VDC to -60 VDC
Max. power consumption of ATCA-7370 (with ATCA-7370-ACC-Module and with RTM-ATCA-737x including 2 SAS HDDs)	260W (typ. 220W)
Max. power consumption of ATCA-7370 (without ATCA-7370-ACC-Module and without RTM)	220W (typ. 180W)
Max. power consumption of ATCA-7370-s (without ATCA-7370-ACCEL-MOD and without RTM)	140W (typ. 120W)

The blade provides two independent power inputs according to the AdvancedTCA Specification. Each input has to be equipped with an additional fuse of max. 90 A located either in the shelf where the blade is installed or the power entry module (PEM).

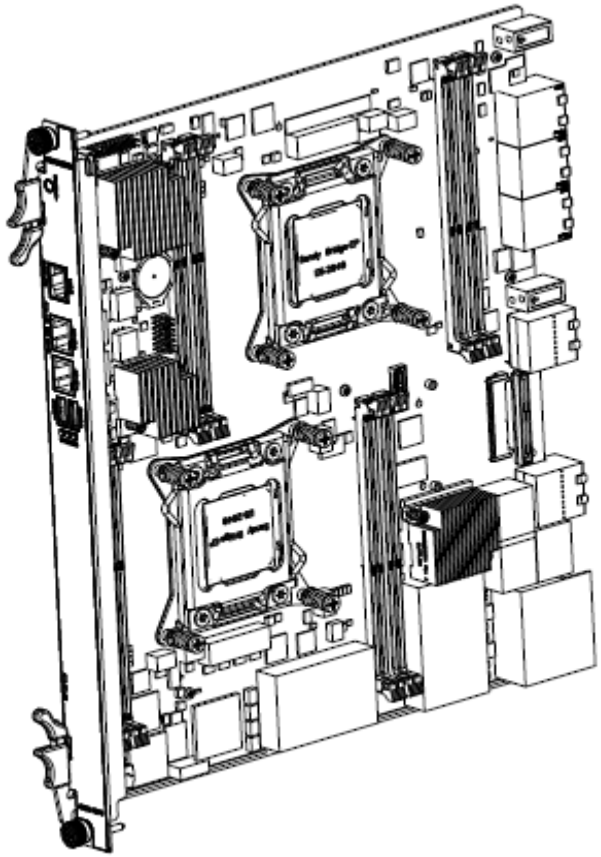
The power consumption has been measured using specific boards in a configuration considered to represent the worst-case (with RTM-ATCA-737x and SAS HDD, maximum memory population, ACC-7370 module) and with software simultaneously exercising as many functions and interfaces as possible. This includes a particular load software provided by Intel designed to stress the processors to reach their theoretical maximum power specification.

Any difference in the system configuration or the software executed by the processors may affect the actual power dissipation. Depending on the actual operating configuration and conditions, customers may see slightly higher power dissipation, or it may even be significantly lower. There is also a dependency on the batch variance of the major components like the processor and DIMMs used. Hence, Artesyn does not represent or warrant that measurement results of a specific board provide guaranteed maximum values for a series of boards.

Note: This power requirement is under room temperature (25^{o}C).

2.3 Blade layout

Figure 2-2 Blade Layout



Note: On the single processor variant the processor and its DIMM sockets are populated on the upper side of the board. Components associated with the second processor are not populated on this product variant.

2.4 Installing the Blade Accessories

The following additional components are available for the blade:

- DIMM memory modules
- Cave Creek module

They are described in detail in the following sections. For order numbers refer to section *Ordering Information* on page 43.

2.4.1 DIMM Memory Modules

The blade provides eight memory slots for main memory DIMM modules. You may install and/or remove DIMM memory modules in order to adapt the main memory size to your needs. The corresponding installation/removal procedures are described in this section.

The location of the DIMM Memory Modules are shown in Figure "Blade Layout" on page 51.

ATCA-7370/ATCA-7370-S supports low-voltage DDR3 memory. This is available upon request.

NOTICE

Damage of Circuits
Electrostatic discharge and incorrect module installation and removal can damage circuits or shorten its life.
Before touching the module or electronic components, make sure that you are working in an ESD-safe environment.

Installation Procedure

To install a DIMM module:

1. Remove blade from system as described in *Installing and Removing the Blade* on page 57.
2. Open locks of memory module socket.
3. Press module carefully into socket.
   As soon as the memory module has been fully inserted, the locks automatically close.
4. If applicable, repeat steps 2 to 3 to install further modules.

NOTICE

Damage of Circuits
Electrostatic discharge and incorrect module installation and removal can damage circuits or shorten its life.
Before touching the module or electronic components, make sure that you are working in an ESD-safe environment.

Removal Procedure

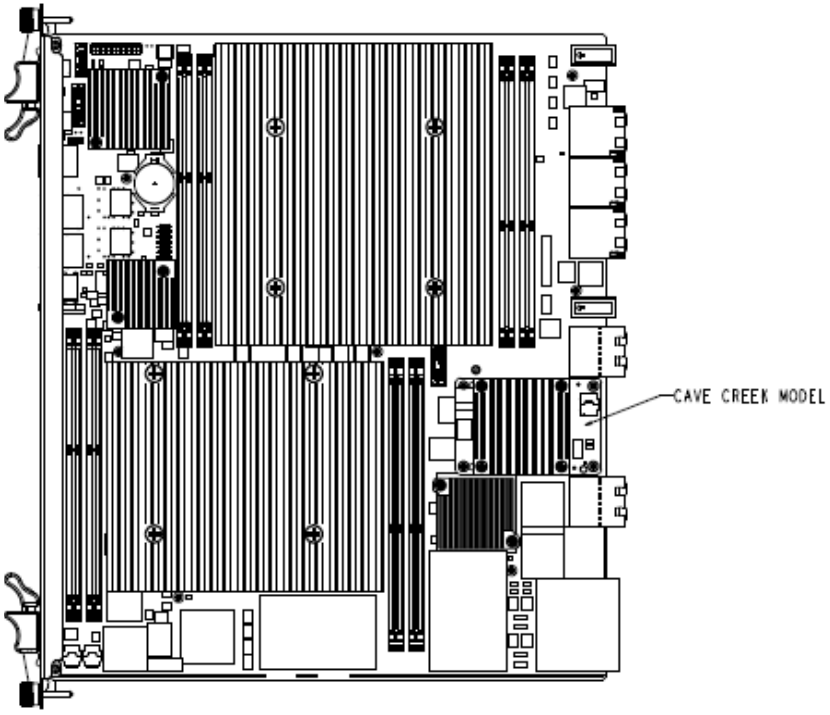
To remove a DIMM module:

1. Remove blade from system as described in *Installing and Removing the Blade* on page 57.
2. Open locks of socket at both sides.
   The memory module is automatically lifted up.
3. Remove module from socket.
4. Repeat steps 2 to 3 in order to remove further memory modules.

2.4.2 Cave Creek Module

This section describes the steps to install/remove the Cave Creek module. The following figure illustrates the location of the Cave Creek module.

Figure 2-3 Cave Creek Module



Note: On the single processor variant the processor and its DIMM sockets are populated on the upper side of the board. Components associated with the second processor are not populated on this product variant.

NOTICE

Damage of Circuits
Electrostatic discharge and incorrect module installation and removal can damage circuits or shorten its life.
Before touching the module or electronic components, make sure that you are working in an ESD-safe environment.

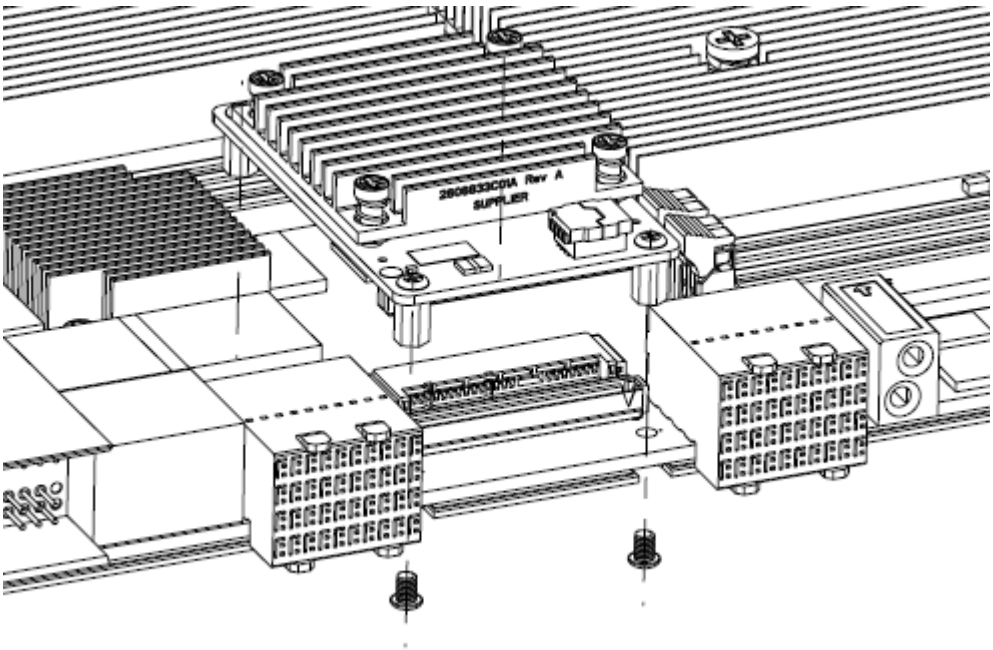
Cave Creek Module Installation

To install the Cave Creek module:

1. Remove the blade from the system as described in *Installing and Removing the Blade* on page 57.
2. Align and fasten the four M2.5x 8mm standoffs from bottom side of Cave Creek module, using the four M2.5x 4mm screws.
3. Insert the Cave Creek module in the socket so that the module's standoffs fit in the blade's mounting holes.

4. Fasten the Cave Creek module to the blade using the four M2.5x 4mm screws.
5. Reinstall the blade into the system as described in *Installing and Removing the Blade on page 57*.

Figure 2-4 Cave Creek Module Installation



Cave Creek Module Removal

To remove the Cave Creek module:

1. Remove the blade from the system as described in *Installing and Removing the Blade on page 57*.
2. Remove the four screws that holds the Cave Creek module.

3. Remove the Cave Creek module from the blade.
4. Reinstall the blade into the system as described in *Installing and Removing the Blade* on page 57.

2.5 Installing and Removing the Blade

The blade is fully compatible to the AdvancedTCA standard and is designed to be used in AdvancedTCA shelves.

The blade can be installed in any AdvancedTCA node slot. Do not install it in an AdvancedTCA hub slot.

NOTICE

Damage of Circuits
Electrostatic discharge and incorrect blade installation and removal can damage circuits or shorten its life.
Before touching the blade or electronic components, make sure that you are working in an ESD-safe environment.

Blade Malfunctioning
Incorrect blade installation and removal can result in blade malfunctioning.
When plugging the blade in or removing it, do not press on the faceplate but use the handles.

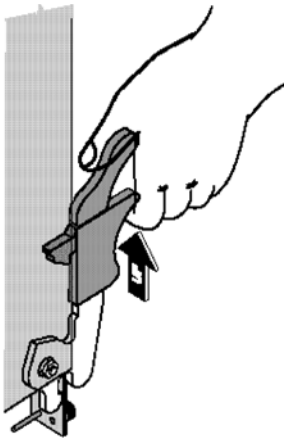
2.5.1 Installing the Blade

To install the blade into an AdvancedTCA shelf, proceed as follows.

Installation Procedure

The following procedure describes the installation of the blade. It assumes that your system is powered on. If your system is not powered on, you can disregard the blue LED and thus skip the respective step. In this case, it is purely a mechanical installation.

1. Ensure that the top and bottom ejector handles are in the outward position by squeezing the lever and the latch together.



2. Insert blade into the shelf by placing the top and bottom edges of the blade in the card guides of the shelf. Ensure that the guiding module of shelf and blade are aligned properly.
3. Apply equal and steady pressure to the blade to carefully slide the blade into the shelf until you feel resistance. Continue to gently push the blade until the blade connectors engage.
4. Squeeze the lever and the latch together and hook the lower and the upper handle into the shelf rail recesses.
5. Fully insert the blade and lock it to the shelf by squeezing the lever and the latch together and turning the handles towards the faceplate.
   If your shelf is powered on, as soon as the blade is connected to the backplane power pins, the blue LED is illuminated.

When the blade is completely installed, the blue LED starts to blink. This indicates that the blade announces its presence to the shelf management controller.

If an RTM is connected to the front blade, make sure that the handles of both the RTM and the front blade are closed in order to power up the blade's payload.

6. Wait until the blue LED is switched off, then tighten the faceplate using the handles, which secures the blade to the shelf.
   The switched off blue LED indicates that the blade's payload has been powered up and that the blade is active.
7. Connect cables to the faceplate, if applicable.

2.5.2 Removing the Blade

This section describes how to remove the blade from an AdvancedTCA system.

NOTICE

Damage of Circuits
Electrostatic discharge and incorrect blade installation and removal can damage circuits or shorten its life.
Before touching the blade or electronic components, make sure that you are working in an ESD-safe environment.

Blade Malfunctioning
Incorrect blade installation and removal can result in blade malfunctioning.
When plugging the blade in or removing it, do not press on the faceplate but use the handles.

Removal Procedure

The following procedure describes how to remove the blade from a system. It assumes that the system is powered on. If the system is not powered on, you can disregards the blue LED and thus skip the respective step. In that case, it is a purely a mechanical procedure.

1. Unlatch the lower handle by squeezing the lever and the latch together and turning the handle outward just enough to unlatch the handle from the faceplate. Do not rotate the handle fully outward.
   The blue LED blinks indicating that the blade power-down process is ongoing.
2. Wait until the blue LED is illuminated permanently, then unlatch the upper handle and rotate both handles fully outward.

If the LED continues to blink, a possible reason may be that the upper layer software rejected the blade extraction request.

NOTICE

Data Loss
Removing the blade with the blue LED still blinking causes data loss.
Wait until the blue LED is permanently illuminated, before removing the blade.

3. Remove the faceplate cables, if applicable.
4. Rotate handle of the faceplate until the blade is detached from the shelf.
5. Remove the blade from the shelf.

Controls, Indicators, and Connectors

3.1 Faceplate

Figure 3-1 shows the connectors, keys and LEDs available at the Faceplate.

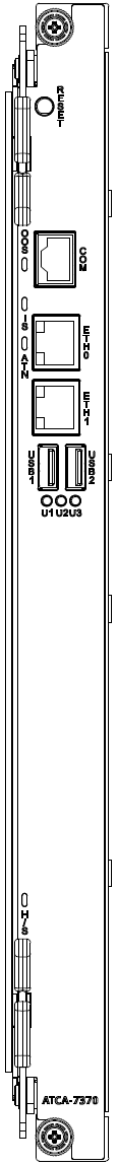
The blade design provides the possibility to cover unused faceplate elements like LEDs or push buttons behind a custom overlay foil.

3.1.1 LEDs and Interfaces

The blade's faceplate provides the following interfaces and control elements:

- Two USB 2.0 ports
- Serial console port to connect to either payload or IPMC serial I/F
- Out of Service, In Service, Attention, User (U1, U2, U3 LEDS) and Hot Swap LEDs (IPMC control)
- Two Ethernet ports
- Recessed reset button

Figure 3-1 Faceplate LEDs



The meaning of these LEDs is described in the following table.

Table 3-1 Faceplate LEDs

Indicator	Color	Description
Out of Service ATCA LED1	Red or Amber	Out of Service Red/ optional Amber (controlled by IPMC): This LED is controlled by higher layer software such as middleware or applications. Red: On after power up and lamp test finished Turned "OFF" by OS startup script or application.
In Service ATCA LED2	Green or Red	In Service Red/green (controlled by IPMC. If both red and green are lit, it may look amber): This LED is controlled by higher layer software such as middleware or applications. Off after power up and lamp test finished Turned green "ON" by OS startup script or application.
Attention ATCA LED3	Amber	Attention Amber: This LED is controlled by higher layer software such as middleware or applications. Off after power up and lamp test finished
Base Ethernet	Green	ON: Link up Blinking: Shows activity OFF: Link down The two LEDs are for the base Ethernet interface and are multiplexed with U1 and U2 using the signal FP_BASE_LED_EN_N signal controlling from FPGA.
U1, U2, U3	Red	User LED ● Red: user defined LED by FPGA register 0x57

Table 3-1 Faceplate LEDs (continued)

Indicator	Color	Description
Hot Swap	Blue	FRU State Machine ● During blade installation – Blue: Onboard IPMC powers up – Blue (blinking): Blade is communicating with the shelf manager – Off: Blade is active ● During blade removal – Blue (blinking): Blade is notifying the shelf manager that it is going to deactivate – Blue: Blade is ready to be extracted

The "Out of service", "In Service" and "Attention" LEDs are directly controlled by IPMC. A higher application software can issue "set/get FRU LED state" command to the IPMC to access them.

3.2 Connectors

3.2.1 Faceplate Connectors

Table 3-2 RJ45 Console Connector Pinout

Pin	Signal
1	RTS
2	DTR
3	TXD
4	GND
5	GND
6	RXD
7	DSR
8	CTS

Table 3-3 USB Connector Pinout

Pin	Signal
1	VP5_USB
2	USB_x_D-
3	USB_x_D+
4	GND

3.2.2 Backplane Connectors

Table 3-4 Zone 1 Connector P1 Pin Assignment

Contact Number	Destination	Description
1 - 4	Reserved	Reserved
5	IPMC ISC PC0	Hardware Address Bit 0
6	IPMC ISC PC1	Hardware Address Bit 1
7	IPMC ISC PC2	Hardware Address Bit 2
8	IPMC ISC PC3	Hardware Address Bit 3
9	IPMC ISC PD4	Hardware Address Bit 4
10	IPMC ISC PD5	Hardware Address Bit 5
11	IPMC ISC PD6	Hardware Address Bit 6
12	IPMC ISC PD7	Hardware Address Bit 7
13	IPMC IMC PD0	IPMB Clock Port A
14	IPMC IMC PD1	IPMB Data Port A
15	IPMC ISC PC5	IPMB Clock Port B
16	IPMC ISC PC4	IPMB Data Port B
17 - 24	Not used	Not used
25	Shelf Ground	Shelf Ground
26	Logic Ground	Logic Ground
27	Power Building Block	Enable B

Table 3-4 Zone 1 Connector P1 Pin Assignment

Contact Number	Destination	Description
28	Power Building Block	Voltage Return A
29	Power Building Block	Voltage Return B
30	Power Building Block	Early -48V A
31	Power Building Block	Early -48V B
32	Power Building Block	Enable A
33	Power Building Block	-48V A
34	Power Building Block	-48V B

Table 3-5 Zone 2 Connector J20 Pin Assignment

J20									
Row #	Interface	Col AB		Col CD		Col EF		Col GH	
1	Backplane Clock	CLK1A+	CLK1A-	CLK1B+	CLK1B-	CLK2A+	CLK2A-		
2	Update Channel SAS & GE Redundancy	UPD_P4_TX+	UPD_P4_TX-	UPD_P4_RX+	UPD_P4_RX-				
3		UPD_P2_TX+	UPD_P2_TX-	UPD_P2_RX+	UPD_P2_RX-	UPD_P3_TX+	UPD_P3_TX-	UPD_P3_RX+	UPD_P3_RX-
4		UPD_GE_TX+	UPD_GE_TX-	UPD_GE_RX+	UPD_GE_RX-	UPD_P1_TX+	UPD_P1_TX-	UPD_P1_RX+	UPD_P1_RX-
5									
6									
7									
8									
9									
10									

Table 3-6 Zone 2 Connector J23 Pin Assignment

J23									
Row #	Interface	Col AB		Col CD		Col EF		Col GH	
1	Fabric Channel 2	F2[2]_TX+	F2[2]_TX-	F2[2]_RX+	F2[2]_RX-	F2[3]_TX+	F2[3]_TX-	F2[3]_RX+	F2[3]_RX-
2		F2[0]_TX+	F2[0]_TX-	F2[0]_RX+	F2[0]_RX-	F2[1]_TX+	F2[1]_TX-	F2[1]_RX+	F2[1]_RX-
3	Fabric Channel 1	F1[2]_TX+	F1[2]_TX-	F1[2]_RX+	F1[2]_RX-	F1[3]_TX+	F1[3]_TX-	F1[3]_RX+	F1[3]_RX-
4		F1[0]_TX+	F1[0]_TX-	F1[0]_RX+	F1[0]_RX-	F1[1]_TX+	F1[1]_TX-	F1[1]_RX+	F1[1]_RX-

Table 3-6 Zone 2 Connector J23 Pin Assignment (continued)

J23									
5	Base Channel 1	BI1_DA+	BI1_DA-	BI1_DB+	BI1_DB-	BI1_DC+	BI1_DC-	BI1_DD+	BI1_DD-
6	Base Channel 2	BI2_DA+	BI2_DA-	BI2_DB+	BI2_DB-	BI2_DC+	BI2_DC-	BI2_DD+	BI2_DD-
7	n/a	NC	NC	NC	NC	NC	NC	NC	NC
8	n/a	NC	NC	NC	NC	NC	NC	NC	NC
9	n/a	NC	NC	NC	NC	NC	NC	NC	NC
10	n/a	NC	NC	NC	NC	NC	NC	NC	NC

Table 3-7 Zone 3 Connector J30 Pin Assignment

J30									
Row #	Interface	Col AB		Col CD		Col EF		Col GH	
1	MISC	COM_TXD	COM_RXD	NC	NC	NC	NCS	PS1_N	RTM_PG
2		SAS2_TX_P	SAS2_TX_N	SAS2_RX_P	SAS2_RX_N	SAS3_TX_P	SAS3_TX_N	SAS3_RX_P	SAS3_RX_N
3		SAS0_TX_P	SAS0_TX_N	SAS0_RX_P	SAS0_RX_N	SAS1_TX_P	SAS1_TX_N	SAS1_RX_P	SAS1_RX_N
4		USB_P	USB_N			SATA_TX+	SATA_TX-	SATA_RX+	SATA_RX-
5									
6	PICE2.0 x4 Port10	PCI-E10_RP[0]	PCI-E10_RN[0]	PCI-E10_TP[0]	PCI-E10_TN[0]	PCI-E10_RP[1]	PCI-E10_RN[1]	PCI-E10_TP[1]	PCI-E10_TN[1]
7		PCI-E10_RP[2]	PCI-E10_RN[2]	PCI-E10_TP[2]	PCI-E10_TN[2]	PCI-E10_RP[3]	PCI-E10_RN[3]	PCI-E10_TP[3]	PCI-E10_TN[3]
8	PCI-E CLOCK	PCI-E10_CLKP	PCI-E10_CLKN	PCI-E_RST	NC	NC	NC	NC	NC
9	MISC	IPMB_L_SCL	IPMB_L_SDA	V3P3_M			PS0_N	RTM_PB_N	RTM_GRST_N
10		V12P	V12P	V12P	V12P	NC	RTM_EN_N	SMB_CLK	SMB_DAT

Table 3-8 Zone 3 Connector J31 Pin Assignment

J31									
Row #	Interface	Col AB		Col CD		Col EF		Col GH	
1	x16 PCIE from CPU1	PCIE_CPU1_RX0+	PCIE_CPU1_RX0-	PCIE_CPU1_TX0+	PCIE_CPU1_TX0-	PCIE_CPU1_RX1+	PCIE_CPU1_RX1-	PCIE_CPU1_TX1+	PCIE_CPU1_TX1-
2		PCIE_CPU1_RX2+	PCIE_CPU1_RX2-	PCIE_CPU1_TX2+	PCIE_CPU1_TX2-	PCIE_CPU1_RX3+	PCIE_CPU1_RX3-	PCIE_CPU1_TX3+	PCIE_CPU1_TX3-
3		PCIE_CPU1_RX4+	PCIE_CPU1_RX4-	PCIE_CPU1_TX4+	PCIE_CPU1_TX4-	PCIE_CPU1_RX5+	PCIE_CPU1_RX5-	PCIE_CPU1_TX5+	PCIE_CPU1_TX5-
4		PCIE_CPU1_RX6+	PCIE_CPU1_RX6-	PCIE_CPU1_TX6+	PCIE_CPU1_TX6-	PCIE_CPU1_RX7+	PCIE_CPU1_RX7-	PCIE_CPU1_TX7+	PCIE_CPU1_TX7-
5		PCIE_CPU1_RX8+	PCIE_CPU1_RX8-	PCIE_CPU1_TX8+	PCIE_CPU1_TX8-	PCIE_CPU1_RX9+	PCIE_CPU1_RX9-	PCIE_CPU1_TX9+	PCIE_CPU1_TX9-

Table 3-8 Zone 3 Connector J31 Pin Assignment

J31									
6		PCIE_CPU1_RX10+	PCIE_CPU1_RX10-	PCIE_CPU1_TX10+	PCIE_CPU1_TX10-	PCIE_CPU1_RX11+	PCIE_CPU1_RX11-	PCIE_CPU1_TX11+	PCIE_CPU1_TX11-
7		PCIE_CPU1_RX12+	PCIE_CPU1_RX12-	PCIE_CPU1_TX12+	PCIE_CPU1_TX12-	PCIE_CPU1_RX13+	PCIE_CPU1_RX13-	PCIE_CPU1_TX13+	PCIE_CPU1_TX13-
8		PCIE_CPU1_RX14+	PCIE_CPU1_RX14-	PCIE_CPU1_TX14+	PCIE_CPU1_TX14-	PCIE_CPU1_RX15+	PCIE_CPU1_RX15-	PCIE_CPU1_TX15+	PCIE_CPU1_TX15-
9	PCIE CLK	CLK_100M_AB+	CLK_100M_AB-	CLK_100M_CD+	CLK_100M_CD-				
10									

Table 3-9 Zone 3 Connector J32 Pin Assignment

J32									
Row #	Interface	Col AB		Col CD		Col EF		Col GH	
1	PCIE Port9	PCIE9_RP[0]	PCIE9_RN[0]	PCIE9_TP[0]	PCIE9_TN[0]	PCIE9_RP[1]	PCIE9_RN[1]	PCIE9_TP[1]	PCIE9_TN[1]
2		PCIE9_RP[2]	PCIE9_RN[2]	PCIE9_TP[2]	PCIE9_TN[2]	PCIE9_RP[3]	PCIE9_RN[3]	PCIE9_TP[3]	PCIE9_TN[3]
3	PCIE Port8	PCIE8_RP[0]	PCIE8_RN[0]	PCIE8_TP[0]	PCIE8_TN[0]	PCIE8_RP[1]	PCIE8_RN[1]	PCIE8_TP[1]	PCIE8_TN[1]
4		PCIE8_RP[2]	PCIE8_RN[2]	PCIE8_TP[2]	PCIE8_TN[2]	PCIE8_RP[3]	PCIE8_RN[3]	PCIE8_TP[3]	PCIE8_TN[3]
5	PCIE Port7	PCIE7_RP[0]	PCIE7_RN[0]	PCIE7_TP[0]	PCIE7_TN[0]	PCIE7_RP[1]	PCIE7_RN[1]	PCIE7_TP[1]	PCIE7_TN[1]
6		PCIE7_RP[2]	PCIE7_RN[2]	PCIE7_TP[2]	PCIE7_TN[2]	PCIE7_RP[3]	PCIE7_RN[3]	PCIE7_TP[3]	PCIE7_TN[3]
7	PCIE Port6	PCIE6_RP[0]	PCIE6_RN[0]	PCIE6_TP[0]	PCIE6_TN[0]	PCIE6_RP[1]	PCIE6_RN[1]	PCIE6_TP[1]	PCIE6_TN[1]
8		PCIE6_RP[2]	PCIE6_RN[2]	PCIE6_TP[2]	PCIE6_TN[2]	PCIE6_RP[3]	PCIE6_RN[3]	PCIE6_TP[3]	PCIE6_TN[3]
9	PCIE CLK	PCIE9_CLKP	PCIE9_CLKN	PCIE8_CLKP	PCIE8_CLKN	PCIE7_CLKP	PCIE7_CLKN	PCIE6_CLKP	PCIE6_CLKN
10		V12P			V12P	V12P	PS0_N		

3.2.3 Mezzanine Card Connector

Table 3-10 Mezzanine Card Connector Signals

D	Signal	C	Signal	B	Signal	A	Signal
1	SMB_SDA	1	SMB_SCI (from IPMC)	1	GBE_Refclk_N	1	GBE_Refclk_P
2	VCC3V3_MGMT	2	GND	2	GND	2	GND
3	CRU_Refclk_N	3	CRU_Refclk_P	3	PCIe_refclk_N	3	PCIe_refclk_P
4	GND	4	GND	4	GND	4	GND
5	PCIe_TX1_N	5	PCIe_TX1_P	5	PCIe_TX0_N	5	PCIe_TX0_P
6	PCIe_RX1_N	6	PCIe_RX1_P	6	PCIe_RX0_N	6	PCIe_RX0_P
7	GND	7	GND	7	GND	7	GND
8	PCIe_TX3_N	8	PCIe_TX3_P	8	PCIe_TX2_N	8	PCIe_TX2_P
9	PCIe_RX3_N	9	PCIe_RX3_P	9	PCIe_RX2_N	9	PCIe_RX2_P
10	GND	10	GND	10	GND	10	GND
11	PCIe_TX5_N	11	PCIe_TX5_P	11	PCIe_TX4_N	11	PCIe_TX4_P
12	PCIe_RX5_N	12	PCIe_RX5_P	12	PCIe_RX4_N	12	PCIe_RX4_P
13	GND	13	GND	13	GND	13	GND
14	PCIe_TX7_N	14	PCIe_TX7_P	14	PCIe_TX6_N	14	PCIe_TX6_P
15	PCIe_RX7_N	15	PCIe_RX7_P	15	PCIe_RX6_N	15	PCIe_RX6_P
16	GND	16	GND	16	GND	16	GND
17		17		17		17	
18	GND	18	GND	18	GND	18	GND
19		19		19		19	
20		20		20		20	
21		21		21		21	
22	GND	22	GND	22	GND	22	GND

Table 3-10 Mezzanine Card Connector Signals (continued)

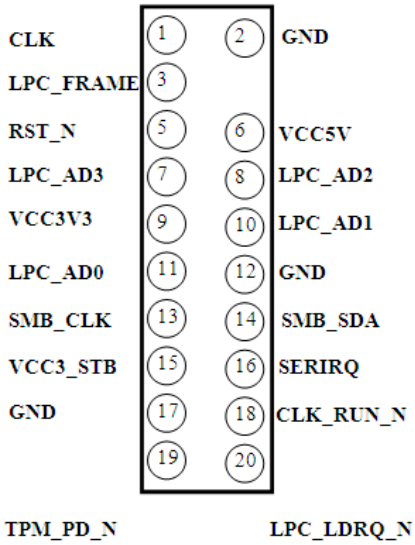
D	Signal	C	Signal	B	Signal	A	Signal
23		23		23		23	
24		24		24		24	
25		25		25		25	
26		26		26		26	
27		27		27		27	
28	RESET_N	28	PRSNT_N	28	PWR_EN	28	PWR_GD
29	VCC12	29	VCC12	29	VCC3V3	29	VCC3V3
30	GND	30	GND	30	GND	30	GND

3.2.4 Onboard Connectors

3.2.4.1 TPM Head

One TPM head is installed on the board and can be used for a Port 80 card for debug monitor. It can also be reserved for a TPM module customization. The head pin pitch is 2.54 mm.

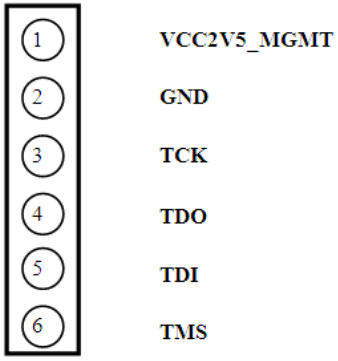
Figure 3-2 TPM Connector Pinout



3.2.4.2 FPGA JTAG Head

A single row six-pin heads for FPGA programming through JTAG is provided on the board.

Figure 3-3 USB 2.0 Flash Disk Module Connector Pinout



3.3 Switch Settings

Switches reside on the component side 1 of the board and are not covered by any other component. Its pin 1 is clearly marked on the PCB and by default are "OFF".

3.3.1 PCH Switch

Table 3-11 Switch SW2 Settings

Switch	PCH	Function	Default
SW2.1	GPIO6	ON: Load default BIOS setting	OFF
SW2.2	GPIO7	ON: BIOS Crisis Recovery	OFF

3.3.2 FPGA Switch

Table 3-12 Switch SW1 Setting

Switch	Function	Default	
SW1.1	Manual power enable of Payload of front board. OFF: IPMC control payload power ON: force payload power on when the board get inserted Note: The S7.1 should also be "ON" in order to force the payload power on.	OFF	
SW1.2	No definition	OFF	
SW1.3	No definition	OFF	
SW1.4	No definition	OFF	

Table 3-13 Switch S7 Setting

Switch	Function	Default	
S7.1	ON: Reset IPMC OFF: IPMC operates normally Note: when forcing board power on or downloading FPGA through cable, the IPMC should be in reset state.	OFF	
S7.2	FPGA image flash BANK selection when using cable to download FPGA image ON: select recovery BANK (U150) OFF: select default BANK (U151)	OFF	

4.1 Features

The Basic Input Output System (BIOS) provides an interface between the operating system and the hardware of the blade. It is used for hardware configuration. Before loading the operating system, BIOS performs basic hardware test, known as power-on self tests (POST) and prepares the blade for the initial boot-up procedure.

During blade production, identical BIOS images are programmed into both boot flash banks. It is possible to select boot flash as device to boot from. This is done via an IPMI command. For further details refer Chapter 8, *Supported IPMI Commands, on page 181*.

The BIOS used on the blade is based on the Phoenix SecureCore Tiano (SCT) UEFI BIOS with several Artesyn extensions integrated. Its main features are:

- Initialize CPU, chipset and memory
- Initialize PCI devices
- Setup utility for setting configuration data
- IPMC support
- Serial console redirection for remote blade access
- Boot operation system

The BIOS complies with the following specifications:

- UEFI Specification 2.0
- Plug and Play BIOS Specification 1.0A
- PCI BIOS Specification 2.1
- SMBIOS Specification 2.3
- BIOS Boot Specification 1.01
- PXE 2.1

- SMP 1.4
- ACPI 4.0

The BIOS contains online documentation which describes in detail the available menu options. Therefore, the description in this manual is limited to the main BIOS functions.

The BIOS setup program is required to configure the blade hardware. This configuration is necessary for operating the blade and connected peripherals. The configuration data are stored in the same flash device from which the board boots.

When you are not sure about configuration settings, restore the default values. This option is provided in case a value has been changed and you wish to reset settings. To restore the default values, press <F9> in Setup.

- Loading the BIOS default values will affect all set-up items and will reset options previously altered.
- If you set the default values, the displayed default values takes effect only after the BIOS setup is saved and closed.

4.1.1 Update and Recovery

The ATCA-7370 has two different ways to update the BIOS.

- Flash tool (FCU and ipmitool in Linux). Used for normal upgrade mode.
- USB CD-ROM or USB flash device. This is used in BIOS recovery modes.

4.1.2 DRAM Support

The BIOS supports the following features of the memory controller:

- Autosizing - The BIOS reads the Serial Presence Detect (SPD) data from the memory modules and automatically configures the chipset accordingly.
- ECC Support
  - Single Bit Errors (SBE) can be detected, corrected and logged. Multi-Bit Errors (MBE) can be detected but not corrected.
  - By default, BIOS enables ECC support in the chipset. However the BIOS setup menu provides an option to enable or disable ECC.
  - ECC Error Report Support: ATCA-7370 supports ECC error reporting. When an ECC error occurs, the memory controller hardware increments an ECC error count and triggers the SMI interrupt to let BIOS or OS handle the ECC error.
  - The ECC counter is cleared at power cycle reset. The counter is preserved during a cold reset, warm reset and S3 suspend/resume.
  - The SMI routine is used to handle ECC error report on both the BIOS and OS. The ECC error log is stored in the BIOS SPI Flash. After Linux is booted up, the Error Detection and Correction Module (EDAC) is also used to count the ECC error.
  - Correctable ECC Logging and Threshold setting in "BIOS setup / Advanced":

Menu Item	Default	Description
Memory ECC Error Log	Both	This item selects the ECC Runtime errors which are to be logged in the SMBIOS event log.
Correctable ECC Logging Threshold	1	This item is used to enter the correctable error threshold value if "Memory ECC Error Log" is not disabled. The logging threshold is based per memory rank, not per DIMM or overall.
Memory Configuration / Correctable ECC Flooding Threshold	100	This item is used to set the error logging limit value per second if "Memory ECC Error Log" is not disabled. If the number of correctable ECC error logs produced per second reaches the flood threshold, the correctable ECC error reporting is disabled. The flood threshold is an overall setting.

Example:
Set threshold to 10.
Given a dual rank DIMM and if 5 errors occur in rank 0 DIMM and 5 errors in rank 1 DIMM, then no ECC event is recorded.
Given a dual rank DIMM and if all the 10 errors occur in one single rank i.e. either rank 0 or rank 1 DIMM, then an ECC event is recorded.

- Available memory space below the 4G boundary - The ATCA-7370 provides 3.25 GB memory space below the 4 GB boundary. The memory map below 4GB is listed in the following table:

Address range	Content
F000_0000 ~ FFFF_FFFF	Flash range RCRB register APIC register etc
E000_0000 ~ EFFF_FFFF	256MB PCIe extend memory space
D000_0000 ~ DFFF_FFFF	PCIe BAR MMIO
0000_0000 ~ CFFF_FFFF	3.25GB available physical memory space

- The memory test is in the Intel Memory Reference Code (MRC) and uses hardware controller intrinsic functions. The MRC is described in the in chapter 7.13 of Intel Xeon Processor E5-1600/2400/2600/4600 Product Families System Agent BIOS Specification 1.01 document (document number 489625).
- Artesyn recommends inserting memory modules of the same type into all slots of the ATCA-7370. With mixed memory, like different model, voltage, or frequency, the system may run in a degraded performance. Though not recommended, a certain combination is possible with the following restrictions:
  - A mix of different sizes
  - A mix of 1.5V and 1.35V modules: all will be configured with 1.5V
  - A mix of 1600MHz and 1333MHz: all will run with 1333MHz

4.1.3 Interrupt Routing

The BIOS provides the interrupt routing to the operating system through the following interfaces:

- PCI IRQ Routing Table (non-ACPI environment)
- Multi Processor Table (non-ACPI environment)
- ACPI_PRT packages (ACPI environment)
- ACPI Multiple APIC Description Table (ACPI environment)

4.1.4 PCI Initialization

The BIOS supports PCI BIOS Specification Revision 2.1.

During power-up self test (POST), the BIOS identifies all PCI-to-PCI bridges and all PCI devices with a header Type 1 in the system. It then initializes them according to their resource requirements.

If the PCI's option ROM is detected, it will be executed and its function implemented. The network option ROM adds new boot option to the BIOS boot table. The SAS option ROM shows SAS configuration utility menu which lets the end user create RAID volume.

4.1.5 I/O Device Configuration

4.1.5.1 Serial Ports

The ATCA-7370 supports two serial ports in OS, but supports only one serial port for console redirection in BIOS. The default value is 3F8h/IRQ4.

4.1.5.2 Integrated SATA Controller

The BIOS provides setup items to configure the embedded serial ATA controller for debugging purposes. Hard disk autotyping is also supported. The BIOS automatically determines the proper geometry for hard disks by reading the information from the drive.

4.1.6 Boot Options

The ATCA-7370 supports BIOS Boot Specification 1.01. The BIOS identifies all IPL (BAID, BEV) devices and BCV devices (hard drives, USB sticks) in the system and will attempt to boot them in the order specified in startup.

The following boot devices are integrated in the BIOS:

- USB devices (sticks, hard drives, CD-ROM)
- Network (BEV)
- SAS HDD connected to C604 chipset
- SATA connected to C604 chipset
- EFI Shell

The default boot order is as follows:

- Attached USB CD-ROM
- Attached USB devices on the external USB port
- SAS HDD
- SATA HDD
- Base Ethernet Interfaces

If BIOS does not find any ready bootable device, it will loop on the source list until a boot device becomes ready. After 10 loops the BIOS initiates a cold reset and retries again or when configured the BMC watchdog bites.

BIOS organizes the devices in groups: CD-ROM, HDD, network, floppy, SAS HDD. Any device can be set as the first boot device by raising it to the first boot device of its device group, then raising that group to the first boot group.

The boot order for a certain device and its device group can be set even in the absence of that device. The order is preserved. When the device is added later, it will be available at the specified boot order.

4.1.6.1 Boot Support for the SAS Controller

The BIOS contains an option ROM SAS controller on the payload. Legacy boot from SAS HDDs is supported.

The ATCA-7370 supports four SAS ports. Two local SAS ports are located in the RTM module, the other two SAS ports are connected to the external ports of the RTM. The SAS physical port number is assigned as follows:

- P0 - Local SAS 1 which is far from RTM zone 3 connector
- P1 - Local SAS 2 which is near from RTM zone 3 connector
- P2 - External SAS 1
- P3 - External SAS 2

The BIOS and Linux follow the SAS port physical number to assign sequence number. For example, BIOS and Linux will assign sequence number as following:

Physical port	BIOS	Linux
P0	SAS0	sda
P1	SAS1	sdb
P2	SAS2	sdc
P3	SAS3	sdd

4.1.6.2 Network Boot

The BIOS contains a classic PXE Option ROM (OpROMs).

The following table summarizes the network boot support status:

Table 4-1 Network Boot Support Status

Ethernet Interface	PXE Boot Support
Base Network Interface 1 (i350 - 1)	YES
Base Network Interface 2 (i350 - 2)	YES
Front Panel Network Interface (i350 - 3)	YES
Update Channel Network Interface (i350 - 4)	No
Fabric Network Interface 1 (82599EB - 1)	YES
Fabric Network Interface 2(82599EB - 2)	YES

4.1.7 I/O Redirection

4.1.8 Console Redirection

Console redirecton or I/O redirection to a COM port allows to configure BIOS through the setup menu even in the absence of a VGA adapter. The following option is configurable through the BIOS setup:

Option	Description
Baudrate	9600 baud, 19200 baud, 38400 baud, and 115200 baud are supported. The default value is 9600.

Serial port 1 is fully compliant to industry standard 16550 asynchronous communication controllers and is integrated in the Glue Logic FPGA.

4.1.9 Serial Over LAN (SOL)

The BIOS writes to an FPGA register in the COM port number where the console redirection is done.

The BIOS sets FPGA register 0x603 bit 0 to high (Serial reduction control register) to indicate the BIOS uses serial port 1 for SOL function. The further steps to initialize SOL is done by IPMC.

4.1.10 IPMI Support

The ATCA-7370 BIOS provides the following IPMI support.

- Checks if the IPMI controller is active. If not, it will display an appropriate error message.
- Reads self-test result from the IPMI controller display. It will display an error message if the self-test fails.
- Sets initial timestamp.
- Sends system firmware progress to the IPMI.
- Logs boot errors to the IPMI event log.

- Sends OS boot events.
- Reads slot information from the IPMI controller and fills the DMI structure Type 1 UUID.

The only supported interface is Keyboard Controller Style (KCS). The IPMI base address and interrupt is provided to OS via SMBIOS structure type38 and is tested with Linux OpenIPMI driver.

4.1.10.1 Watchdogs

The watchdogs in ATCA-7370 are implemented by BMC watchdog.

BIOS uses BMC watchdog in two phases.

- BIOS phase
- OS phase

BMC watchdog for BIOS phase is started by the BMC automatically after the payload board is powered on. BIOS can disable BMC watchdog through the BIOS setup menu. If BMC watchdog for BIOS is enabled, it will be disabled when BIOS setup menu is invoked boot to shell or boot to OS. Timer value for BIOS phases is also configurable through BIOS setup menu. The default time value is set to three minutes and the BMC watchdog for BIOS phase is enabled by default.

The BIOS can disable the BMC watchdog for OS loading phases through the BIOS setup. Timer value for OS loading phases is also configurable through BIOS setup. The default timer value is five minutes, and the BMC watchdog for OS phase is disabled by default.

If BMC watchdog times out in the BIOS phase, BMC will switch the BIOS bank.

4.1.11 SMBIOS Support

The BIOS includes SMBIOS structures according to SMBIOS 2.4 and IPMI1.5 specifications.

4.1.12 LED Behavior During POST

After power up/reset and while BIOS runs the LEDs are used to signalize the power up/ BIOS phases. The state of LEDs is defined so that in case of a hang, the LEDs clearly indicate in which boot up phase the hang occurred. In general, to indicate that the POST is in progress, the BIOS toggles the user LED for every POST task it executes. After the POST has been completed, the BIOS switches off the LEDs. The LEDs marked with B1/U1,B2/U2 and U3 will be used for this purpose.

4.1.13 BIOS Setup Layout

The BIOS Setup default is aligned with the ATCA-7370 BIOS defaults.

4.1.13.1 Board Information Display

The BIOS displays the following board related information in the BIOS setup under "Board Info".

- Current System (label for the loaded BIOS defaults set)
- BIOS version
- BIOS build date
- IPMI Firmware Version
- FPGA Version (Onboard FPGA version)
- BIOS Source (boot flash device bank)

4.1.14 USB 2.0 Ports

The ATCA-7370 supports three external 2.0 ports. All USB ports support low-speed, full-speed and high-speed using the USB 2.0 Enhanced Host Controller Interface (EHCI).

4.1.15 Supported Operating Systems

The following operating systems are supported by the ATCA-7370. DOS is used for debugging.

- WRS PNE LE 4.3 Linux and higher
- Red Hat Enterprise Linux 6.x

4.1.16 SPI Boot Flash

The SPI boot flash contains a descriptor mode image with all required parameters as described in Intel®Patsburg chipset SPI Flash Programming Guide Revision 1.6 (Intel Confidential)

4.1.17 Serial Console and BIOS Printouts

The BIOS initializes the serial port and uses the serial port as output console. The default settings for the serial port are: 9600 bps, 8 data bits, no parity, 1 stop bits, no flow control.

The BIOS printout does not cause any significant delay to boot up. Default terminal emulation is VT-100. The ATCA-7370 vendor, Phoenix, specifies and documents the terminal hot keys and keystroke mapping for VT-100, ANSI and VT-UTF8.

The BIOS prints all errors found during BIOS phase. In addition to errors, BIOS prints the information contained in the Board Information to console.

4.1.17.1 BIOS Printouts to DRAM

BIOS console printouts are stored in a specific area of the DRAM. The printouts are accessible by the OS, allowing the use of the startup information for debugging and troubleshooting. Storing the optional ROM printouts is not required. All printouts from the serial console are logged into the DRAM buffer.

A simple structure is used to locate the printouts buffer and define its size. This floating structure is located between addresses E000h and FFFFFh.

Table 4-2 Printout Floating Structure

Field	Offset (in bytes:bits)	Length (in bits)	Description
SIGNATURE	0	32	The ASCII string represented by "_CP_" which serves as a search key for locating the pointer structure.
VERSION	4	16	Version (low byte = minor, high byte = major). Version 1.00 (0100h) is defined.
PHYSICAL ADDRESS POINTER	6	32	The address of the beginning of the CP table. All zeros if the CP table does not exist.
BUFFER SIZE	10	16	Printouts buffer size in bytes.

Table 4-2 Printout Floating Structure (continued)

Field	Offset (in bytes:bits)	Length (in bits)	Description
LENGTH	12	8	The length of the floating pointer structure table in bytes. The version 1.00 structure is 14 bytes long; so this field contains 0Eh.
CHECKSUM	13	8	A checksum of the complete pointer structure. All bytes specified by the length field, including CHECKSUM and reserved bytes, must add up to zero.

4.1.18 BIOS Interface towards OS

4.1.18.1 Proprietary BIOS Data Area (BDA) Bytes

BIOS provides control for warm or cold reset types through the BIOS Data Area (BDA). The following BDA bytes are required by the OS.

40:00	I/O addresses of four COM ports
40:72	BIOS warm reset flag.
40:D0	BIOS warm reset counter.

4.1.18.2 BIOS CLI Tool - IPMIBPAR

The IPMIBPAR tool can be used to change the IPMI Boot Parameter list when Linux is up and running. It supports the following options.

Table 4-3 BIOS CLI Tool - IPMIBPAR

Option	Description
-d	Enable debug output
-a xx	IPMB Address, if not present local IPMC is used
-i	Get device ID
-g	Get IPMI Boot Parameter USER area

Table 4-3 BIOS CLI Tool - IPMIBPAR

Option	Description
-s file	Store IPMI Boot Parameter (USER area), read from file
-h	Help

4.2 Setup Utility

The BIOS incorporates a Setup utility that allows you to alter a variety of system options. This section describes the operation of the Setup utility, which explains the various options available through a set of hierarchical menus. All options are not available with the product, and some options depend on BIOS customizations.

The current settings are stored in the NVRAM area, and any changes can be copied back to this area through the Exit menu.

To start the Setup utility, press <F2> key during the early stages of POST after the power up.

This functionality operates when the USB keyboard is enabled, and through the console redirection facility enabled.

The following table briefly describes the Primary Menus options, and most of the Primary Menus have sub-menus.

Table 4-4 Primary Menu Description

Menu	Options
Main	Provides system information, date, and time
Advanced	Advanced features including Boot, Processor, Peripheral, USB, Memory, South Bridge and SMBIOS event log settings.
Security	Supervisor and User password options.
Boot	Boot priority order.

Table 4-4 Primary Menu Description (continued)

Menu	Options
Exit	Save with or without changes, Loads or saves default settings.

The Phoenix SecureCore Tiano (SCT) navigation can be accomplished using a combination of the keys. These keys include the function keys, Enter, Esc, Arrow keys, etc.,. The following table describes the SCT navigation keys.

Table 4-5 SCT Navigation Keys

Key	Description
ENTER	The Enter key allows to select an option, to edit its value or access a sub-menu.
>< Left/Right	The Left and Right <Arrow> keys allow to select a screen or menu. For example, Main screen, Advanced screen, Exit screen, etc.,.
^v Up/Down	The Up and Down <Arrow> keys allow to select an item or sub-screen.
+- Plus/Minus	The Plus and Minus keys allow to change the field value of a particular setup item. For example, Date and Time.
Tab	The Tab key allows to select fields.
ESC	The Esc key allows to discard any changes made and exit the SCT Setup. When you are in a submenu, The Esc key allows you to exit to the upper menu.
Function keys	When other function keys become available, they are displayed at the right of the screen along with their intended function.
F1	General Help
F9	Load Optimized Defaults
F10	Save ESC and Exit

4.2.1 Main Menu

Figure 4-1shows the Main Menu options.

Figure 4-1 Main Menu

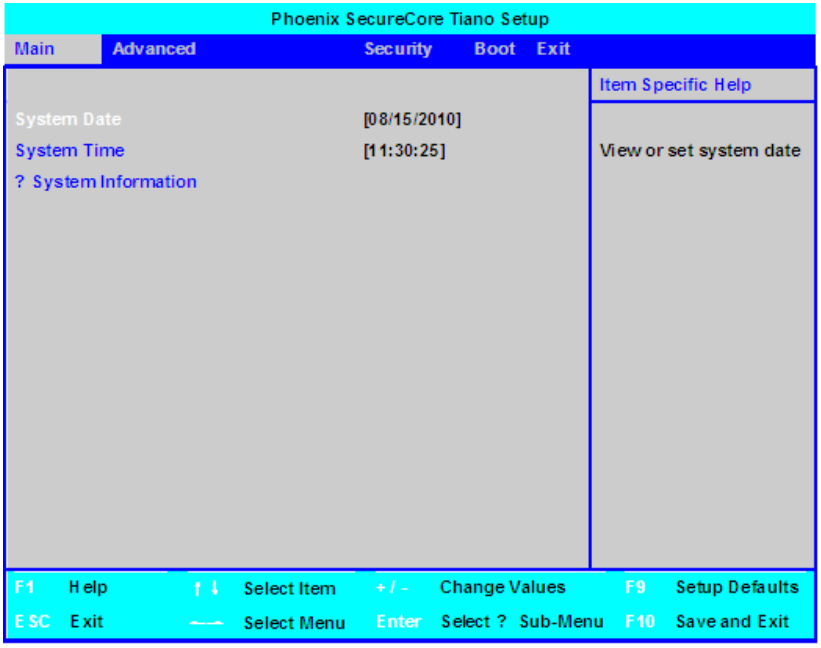


Table 4-6 Main Menu Description

Field	Description
System Date	Sets the time and date (month/day/year format). To change these values, go to each field and enter the desired value. Press the <Tab> key to move from hour to minute, minute to second, month to day, or day to year. There is no default value.
System Time	
System Information	Gives the BIOS version, CPU type, memory type size, etc.,

4.2.2 Advanced Menu

Figure 4-2 shows the Advanced Menu options.

Figure 4-2 Advanced Menu

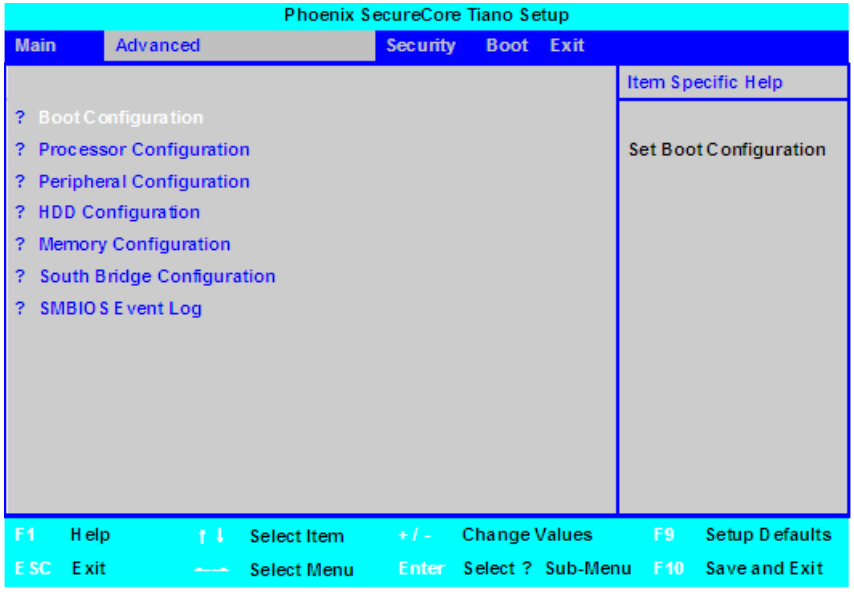


Table 4-7 Advanced Menu Description

Field	Description
Boot Configuration	Set boot configuration. See section *Boot Configuration*
Processor Configuration	Set CPU configuration. See section *Processor Configuration*
Peripheral Configuration	Set system peripheral configuration. See section *Peripheral Configuration*.
HDD Configuration	Set hard drive and controller configuration. See section *HDD Configuration*.
Memory Configuration	Displays and provides options to change the memory settings. See section *Memory Configuration*.
South Bridge Configuration	Set south bridge configuration. See section *South Bridge Configuration*.

Table 4-7 Advanced Menu Description (continued)

Field	Description
SMBIOS Event Log	Set SMBIOS configuration. See section *SMBIOS Event Log*.

4.2.2.1 Boot Configuration

Table 4-8 lists the Boot Configuration options.

Table 4-8 Boot Configuration Description

Field	Description
System Reset Type	Enable Warm Reset support, which controls next reset type. Set to "Cold Reset", to change next reset type to cold reset; Set to "Warm Reset", to change next reset type to warm reset. Options: Warm Reset and Cold Reset. Default is Warm Reset.
Warm Reset Counter	Sets the default value of Warm Reset Counter. Range: 0 ~ 65535. Default is 5.
RPB Terminal Type	Emulation: ANSI: Extended ASCII char set. VT100: ASCII char set. VT100+: Extends VT100 to support color, function keys, etc. UTF8: Uses UTF8 encoding to map Unicode chars onto 1 or more bytes. Options: ANSI, VT100, VT100+ and UTF8. Default is VT100.
RPB Baudrate	Selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds. Options: 9600, 19200, 38400, 57600 and 115200. Default is 9600.
Front Network Boot	Controls execution of the Option ROM for the Front Panel Ethernet controller. Options: Disabled and Enabled. Default is Disabled.

Table 4-8 Boot Configuration Description (continued)

Field	Description
Base Network Boot	Controls execution of the Option ROM for the Base Ethernet controller. Options: Disabled and Enabled. Default is Enabled.
Fabric Network Boot	Controls execution of the Option ROM for the Fabric Interface Ethernet. Options: Disabled and Enabled. Default is Disabled.
ARTM Network Boot	Controls execution of the Option ROM for the Ethernet on the ARTM. Options: Disabled and Enabled. Default is Disabled.
ARTM SAS Boot	Controls execution of the Option ROM for the SAS controller on the ARTM. Options: Disabled and Enabled. Default is Enabled.
Boot from USB Devices	Enable or Disable booting from USB Devices. Options: Disabled and Enabled. Default is Enabled.
BIOS Watchdog	Enable or Disable BIOS POST Watchdog. Options: Disabled and Enabled. Default is Enabled.
BIOS Watchdog Timeout	Choose Timeout value for BIOS POST Watchdog Expiration value. It is not available if the BIOS Watchdog is disabled. Range: 180 ~ 6000. Default is 180.
O/S Boot Watchdog	Enable or Disable O/S Watchdog Timer. It is not available if the O/S Watchdog is disabled. Options: Disabled and Enabled. Default is Disabled.
O/S Boot Watchdog Timeout	Choose Timeout value for O/S Boot Watchdog Timer. Range: 180 ~ 6000. Default is 300.

4.2.2.2 Processor Configuration

Table 4-9 lists the Processor Configuration options.

Table 4-9 Processor Configuration Description

Field	Description
Active Processor Cores	Number of cores to enable in each processor package. Options: ALL, 1, 2, 3, 4, 5, 6, 7. Default is ALL.
Intel(R) HT Technology	Enabled for Windows XP and Linux (OS optimized for Hyper-Threading Technology) and Disabled for other OS (OS not optimized for Hyper-Threading Technology). When disabled, only one thread per enabled core is enabled. Options: Disabled and Enabled. Default is Disabled.
CPU Flex Ratio Override	Enable or Disable CPU Flex Ratio Programming. Option: Disabled and Enabled. Default is Disabled.
CPU Flex Ratio Settings	Allows for selecting the CPU Ratio value, this value must be between Max efficiency ratio and Max non-turbo ratio. Range: 12 ~ 30. If "CPU Flex Ratio Override" is disabled, the CPU Flex Ratio Settings menu item is hidden. To view this menu item set "Advanced > Processor Configuration > CPU Flex Ratio Override" to enable. Default is 18.
Enabled XD	Enabled Execute Disabled functionality. Also known as Data Execution Prevention (DEP). Options: Disabled and Enabled. Default is Disabled.
Intel(R) Virtualization Technology	When enabled, a VMM can utilize the additional hardware capabilities. Options: Disabled and Enabled. Default is Enabled.
Intel(R) SpeedStep(tm)	Enable processor performance states (P-States). Options: Disabled and Enabled. Default is Enabled.
Turbo Mode	Enable Processor Turbo Mode. TM must also be enabled. Options: Disabled and Enabled. Default is Disabled.

Table 4-9 Processor Configuration Description (continued)

Field	Description
C-States	Enable processor idle power saving states (C-States). Options: Disabled and Enabled. Default is Enabled.

4.2.2.3 Peripheral Configuration

Table 4-10 lists the Peripheral Configuration options.

Table 4-10 Peripheral Configuration Description

Field	Description
Spread Spectrum Clock	Enable/Disable Spread Spectrum. Options: Disabled and Enabled. Default is Enabled.
RTM power policy	Select RTM power policy. Disable for RTM as an independent FRU, or enable for RTM Activate/Deactivate with front board. Options: Disabled and Enabled. Default is Disabled.

4.2.2.4 HDD Configuration

Table 4-11 lists the HDD Configuration options.

Table 4-11 HDD Configuration Description

Field	Description
SATA Interface Combination	Select the SATA controllers operation mode. Options: IDE and AHCI. Default is AHCI.
Serial ATA Port 0 / Hard Disk 0	Displays the identity of the device attached.
Serial ATA Port 1 / Hard Disk 1	Displays the identity of the device attached.
Serial ATA Port 2 / Hard Disk 2	Displays the identity of the device attached.
SAS HDD 1	Displays the identity of the device attached.

Table 4-11 HDD Configuration Description

Field	Description
SAS HDD 2	Displays the identity of the device attached.
SAS HDD 3	Displays the identity of the device attached.
SAS HDD 4	Displays the identity of the device attached.

4.2.2.5 Memory Configuration

Table 4-12 lists the Memory Configuration options.

Table 4-12 Memory Configuration Description

Field	Description
DDR Refresh	Allows override selection of the DDR3 refresh rate for normal operation. Options: Auto, 7.8us and 3.9us. Default is Auto.
DDR Vdd Limit	Select DDR Vdd voltage. When DDR Vdd Limit is set to 'auto', then based-on the following conditions the memory voltage can be either 1.5V or 1.35V: - If all memory modules support 1.5V, then the BIOS set memory voltage to 1.5V. - If all memory modules support 1.35V, then the BIOS set memory voltage to 1.35V. - If some of the memory module support 1.35V and other support 1.5V, then the BIOS set memory voltage to 1.5V. Options: Auto and 1.5V. Default is Auto.
ECC Support	Error Correction And Checking (ECC) mechanism support. Options: Disabled and Enabled. Default is Enabled.
Memory ECC Error Log	Select ECC Runtime errors type to be logged in SMBIOS event log. Select type include Correctable Error (CE), Uncorrectable Error (UC), both CE and UC error (Both). Options: Disabled, CE, UC, and Both. Default is Both.

Table 4-12 Memory Configuration Description (continued)

Field	Description
Correctable ECC Logging Threshold	Enter the correctable error threshold value if Runtime Error Logging option is enabled. Range: 1 ~ 32767. Default is 1.
Correctable ECC Flooding Threshold	Enter the Error Logging Limit value if Runtime Error Logging option is enabled. Range: 1 ~ 65535. Default is 20.

4.2.2.6 South Bridge Configuration

Table 4-13 lists the South Bridge Configuration options.

Table 4-13 South Bridge Configuration Description

Field	Description
SB USB Config	Set USB configuration. See *SB USB Configuration*.

4.2.2.6.1 SB USB Configuration

Table 4-14 lists the SB USB Configuration options.

Table 4-14 SB USB Configuration Description

Field	Description
USB1 Control	Enable or disable Front Panel USB port 1. Options: Disabled and Enabled. Default is Enabled.
USB2 Control	Enable or disable Front Panel USB port 2. Options: Disabled and Enabled. Default is Enabled.
RTM USB Control	Enable or disable RTM USB port. Options: Disabled and Enabled. Default is Enabled.

4.2.2.7 SMBIOS Event Log

Table 4-15 lists the SMBIOS Event Log options.

Table 4-15 SMBIOS Event Log Description

Field	Description
Event Log	Enable or disable SMBIOS Event Log. Option: Disabled and Enabled. Default is Enabled.
View SMBIOS event log	View SMBIOS event log.
Mark SMBIOS events as read	Mark SMBIOS events as read. Marked SMBIOS events will not be displayed.
Clears SMBIOS events	Clears SMBIOS events.

4.2.3 Security Menu

Figure 4-3 shows the Security Menu options.

Figure 4-3 Security Menu

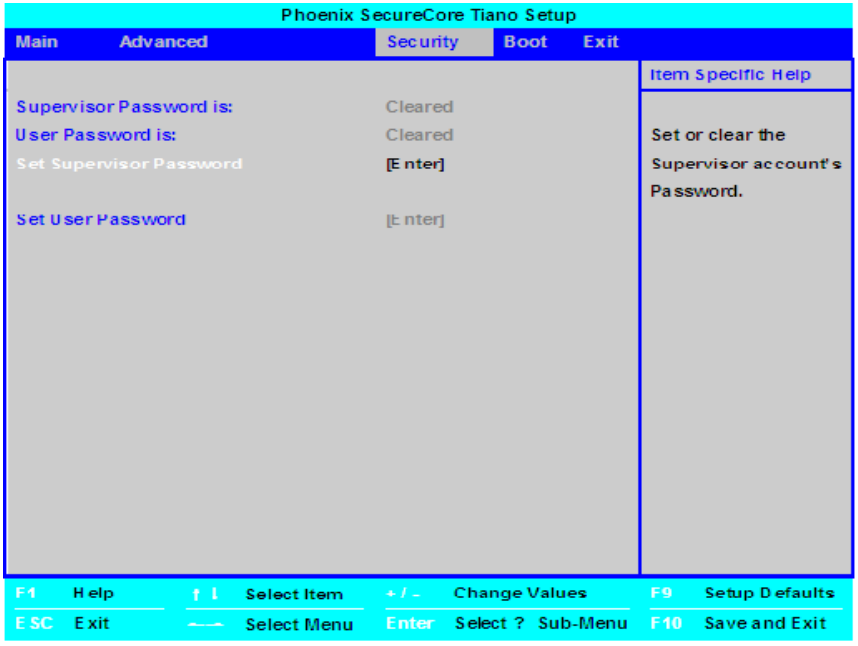


Table 4-16 Security Menu Description

Field	Description
Set Supervisor Password	Set Setup Supervisor Password.
Set User Password	Set Setup User Password.

4.2.4 Boot Menu

Figure 4-4 shows the Boot Menu options.

Figure 4-4 Boot Menu

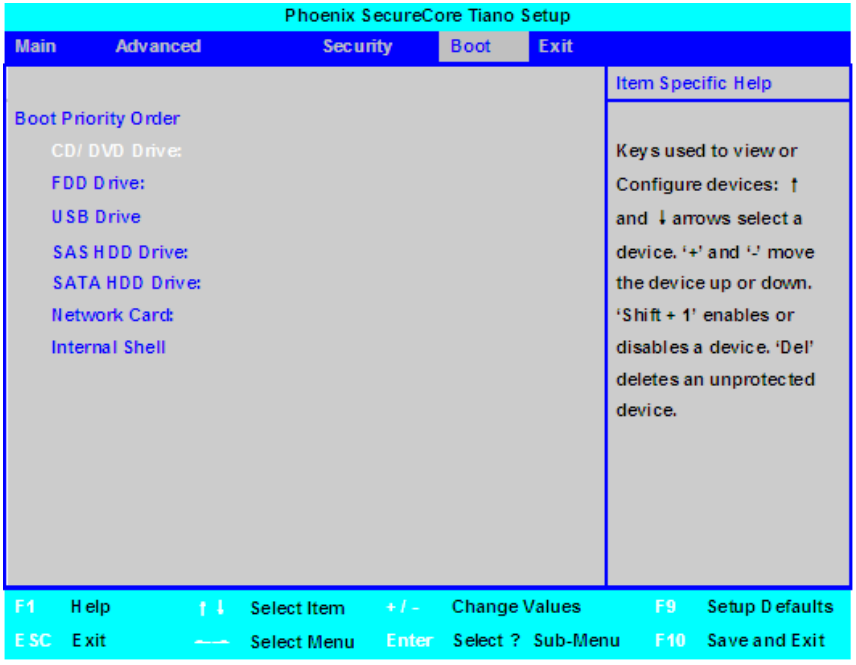

Phoenix SecureCore Tiano Setup
Main
Advanced
Security
Boot
Exit
Item Specific Help
Boot Priority Order
CD/ DVD Drive:
FDD Drive:
USB Drive
SAS HDD Drive:
SATA HDD Drive:
Network Card:
Internal Shell
Keys used to view or Configure devices: ↑ and ↓ arrows select a device. '+' and '-' move the device up or down. 'Shift + 1' enables or disables a device. 'Del' deletes an unprotected device.
F1 Help
↑ ↓ Select Item
+ / - Change Values
F9 Setup Defaults
ESC Exit
← → Select Menu
Enter Select ? Sub-Menu
F10 Save and Exit

Table 4-17 Boot Menu Description

Field	Description
Boot Priority Order	Sets the order of the devices group.
CD/ DVD Drive	Sets the order of the CD/ DVD devices in CD/ DVD group.
FDD Drive:	Sets the order of the USB floppy drive devices in floppy group.
USB Drive	Sets the order of the USB HDD devices in USB group.
SAS HDD Drive	Sets the order of the SAS HDD devices in SAS HDD group.
SATA HDD Drive	Sets the order of the SATA HDD devices in SATA HDD group.

Table 4-17 Boot Menu Description (continued)

Field	Description
Network Card	Sets the order of the Network Card devices in Network Card group.
Internal Shell	Sets the order of internal UEFI shell.

4.2.5 Save and Exit Menu

Figure 4-5 shows the Save and Exit Menu options.

Figure 4-5 Save and Exit Menu

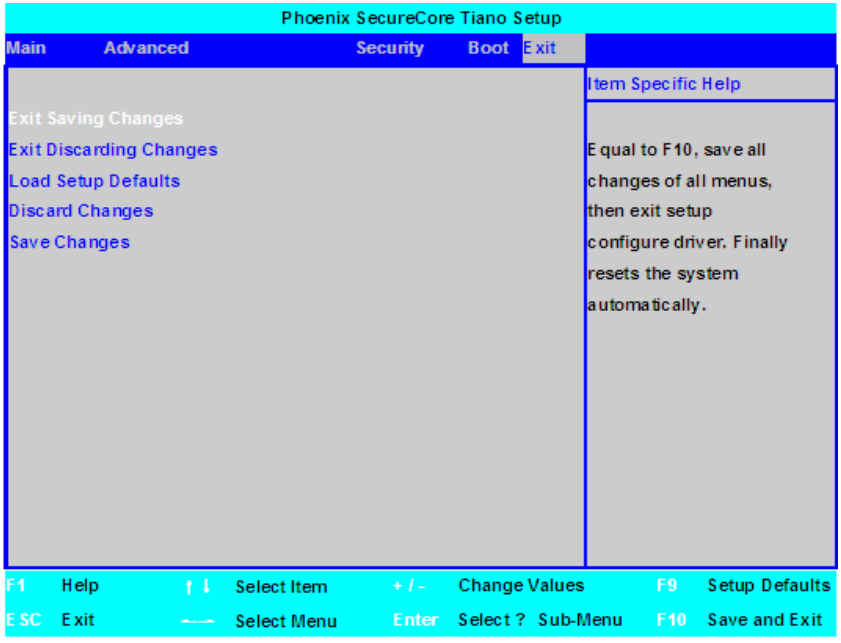


Table 4-18 Save and Exit Menu Description

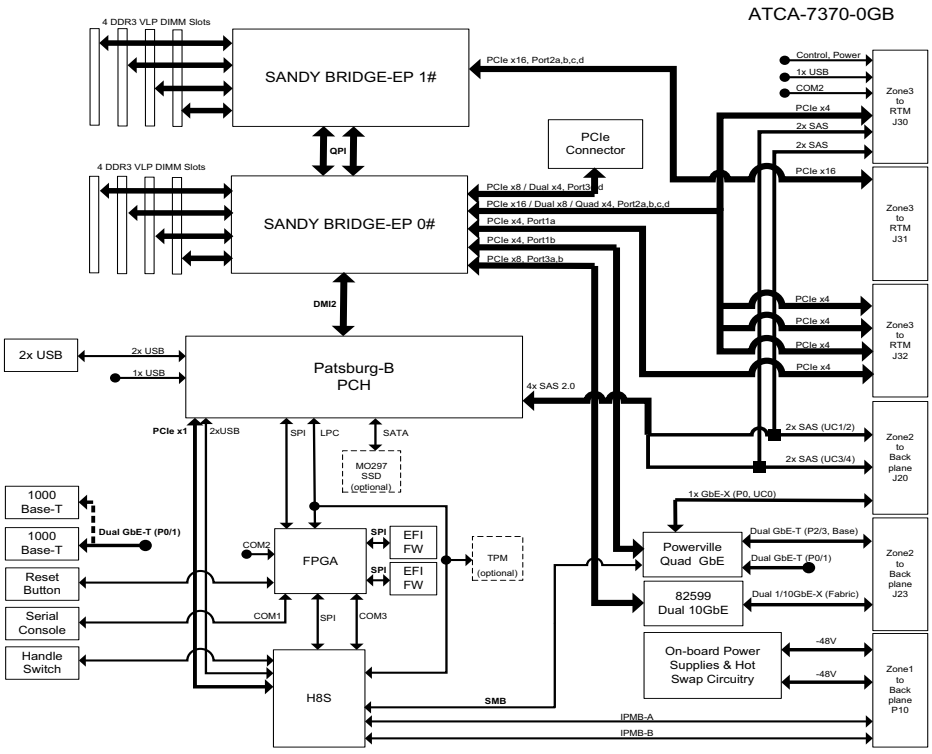
Field	Description
Exit Saving Changes	This option is same as pressing <F10> key. Saves all changes of all menus, then exits the setup configure driver. The option finally resets the system automatically.

Table 4-18 Save and Exit Menu Description (continued)

Field	Description
Exit Discarding Changes	This option is same as pressing <ESC> key. It does not save changes, and then exits setup configure driver. Finally resets the system automatically.
Load Setup Defaults	This option is same as pressing <F9> key. Loads standard default values.
Discard Changes	Loads the original value of the boot time, but does not load the default setup value.
Save Changes	Saves all changes of all menus, but does not reset the system.

5.1 Block Diagram

Figure 5-1 Block Diagram



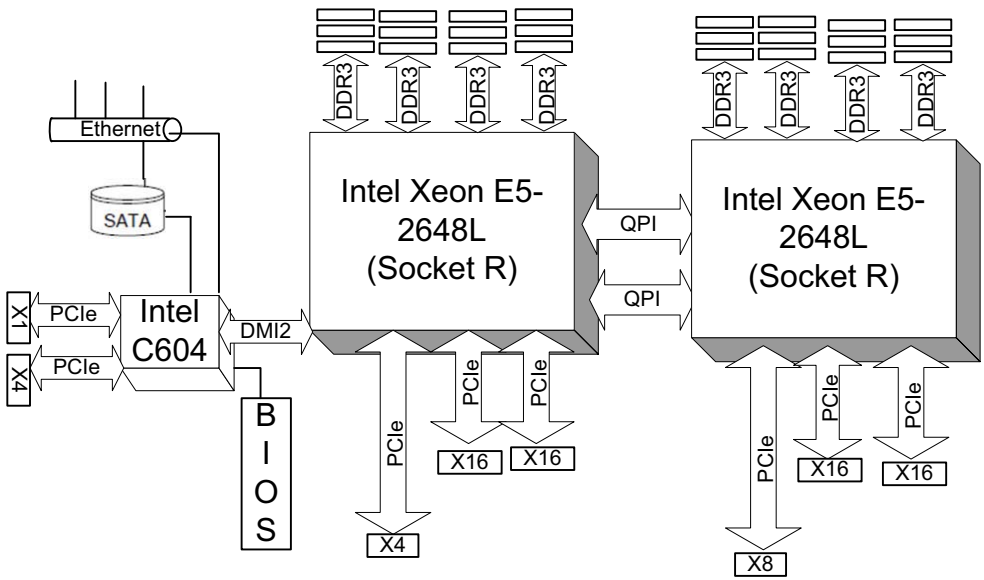
Note: On the single processor variant the processor and its DIMM sockets are populated on the upper side of the board. Components associated with the second processor are not populated on this product variant.

5.2 Processor

The Intel Xeon E5-2648L Processor is an eight-core processor, based on 32 nm process technology with LGA 2011 package (Socket R). The processor features two Intel Quick Path Interconnect point-to-point links capable of up to 8.0 GT/S, 20 MB of shared Last Level cache (L3), 40 Lanes Gen3 PCIe and four channels Integrated Memory Controller (IMC). The processor support all the existing Streaming SIMD Extensions 2 (SSE2), Streaming SIMD Extensions 3 (SSE3) and Streaming SIMD Extensions 4 (SSE4). The processor supports several Advanced Technologies: Execute Disable Bit, Intel 64 Technology, Enhanced Intel SpeedStep Technology, Intel Virtualization Technology, and Simultaneous Multi Threading (SMT).

The following figure shows the Intel Xeon E5-2648L processor block diagram.

Figure 5-2 Intel Xeon Processor E5-2648L/C604 Chipset Platform Overview



Note: On the single processor variant the processor and its DIMM sockets are populated on the upper side of the board. Components associated with the second processor are not populated on this product variant.

5.3 Memory

5.3.1 DDR3 Main Memory

ATCA-7370 provides a dual Intel Xeon Processor E5-2648L CPU with Integrated Memory Controller (IMC). Each IMC supports four independent 72-bit (64-bit Data + 8-bit ECC) wide DDR3 memory channels.

ATCA-7370 supports one VLP DIMM sockets for each memory channel resulting in a total of eight DDR3 DIMM sockets.

Supported DDR3 speeds are DDR3-800, DDR3-1066, DDR3-1333 and DDR3-1600. DDR3 signaling voltage level is 1.35 V/1.5 V. Higher DDR3 memory speed may be supported by the next generation processor.

5.4 Network

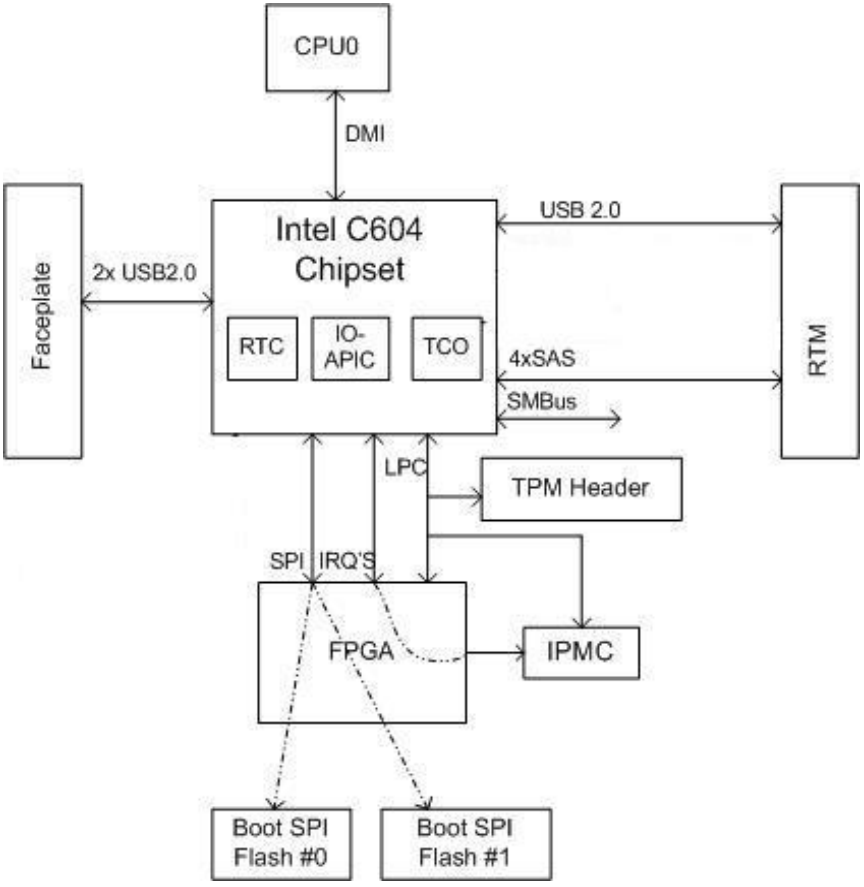
5.5 I/O Controller

Intel C604 chipset is PCH that is used with Intel Xeon E5-2648L Processor. It provides the following interfaces:

- x4 lane DMI connect to CPU
- Eight lanes PCIe Gen2
- Four ports SAS
- Six serial ATA (SATA) interfaces
- Fourteen USB 2.0 interfaces
- SPI Interface for BIOS
- 32-bit PCI Interface
- SM bus

The following figure shows the I/O functions provided by C604 chipset and those used on ATCA-7370/ATCA-7370-S.

Figure 5-3 PCH Block Diagram



5.6 Ethernet Ports

5.6.1 ATCA 3.0 Base Interface

The dual Base interface of the ATCA-7370 Node board is from two ports of Intel I350 quad ports Gigabit Ethernet Controller. The device offers quad 10/100/1000Base-T and quad 1000Base-X interfaces. A serial EEPROM is used for storage of configuration parameters such as the MAC addresses.

The two 10/100/1000Base-T interfaces of the Intel I350 are directly connected to the transformers and providing the ATCA Base interface on connector P23 rows #5 and #6 (Node Board). This redundant connection provides the Dual-Star Base Interface configuration required according to ATCA 3.0 specification (Base Interface is always Dual Star 10/100/1000Base-T).

5.6.2 Fabric Interface ATCA 3.1

The ATCA-7370 Fabric Interface is provided by Intel 82599 (Niantic). It is in accordance to ATCA subsidiary specification 3.1 Ethernet for ATCA Systems. Either two10GBase-BX4 or two 1000Base-BX Ethernet interfaces are connected to the fabric channel #1 and #2 in the Zone 2 providing support for ATCA 3.1 Option 1 and 9.

- Option 1 (one 1000Base-BX on Port 0 of the fabric channels 1,2)
- Option 9 (one 10GBase-BX4 on Port 0-3 of the fabric channels 1,2)

The two 10GBase-BX4 and the two 1000Base-BX interfaces are connected to the ATCA backplane's Fabric Interface on connector P23 rows #4,#3 (Fabric Channel 1 Port 0-3) and rows #2,#1 (Fabric Channel 2 Port 0-3)

5.6.3 Faceplate Ethernet Ports

The ATCA-7370 provides two RJ45 on its front panel for Gigabit Ethernet. The RJ45-0 (the lower one on front panel) can support 10/100/1000 BASE-T ethernet. The RJ45-1(the lower one on front panel) share the same controller in I350 with update channel GE interface. The update channel is active currently, so the RJ45-1 is reserved and cannot been used now.

5.6.4 Update Channel Ethernet

The ATCA-7370 supports one Gigabit Ethernet on update channel on P20 of Zone2 connector. It uses SerDes interface and occupies the port 0 of update channles.

5.7 Storage

ATCA-7370 supports the following types of storage:

- Front panel USB DISK (up to two ports)
- Storage RTM with SATA/SAS support

5.8 IPMC

The blade features an Intelligent Platform Management Controller (IPMC) compliant to PICMG 3.0 and IPMI 1.5 and 2.0 (SOL only). The IPMC is a management subsystem providing monitoring, event logging, and recovery control. The IPMC serves as the gateway for management applications to access the payload hardware.

The IPMC firmware (FW) is stored in two independent memory images. Crisis recovery control is provided to allow reboot of the IPMC from a second image if the upgraded FW image is corrupted. FW images can be upgraded via HPM.1/IPMI using either IPMB or KCS interface.

The IPMC supports the initiation of a graceful shutdown of the host CPU. The IPMC can force the CPU to reset. It also controls the power and reset of the payload.

The IPMC provides a watchdog that supervises the payload. If enabled, the payload software needs to retrigger the Watchdog to prevent time-out. A watchdog time-out can generate a NMI, a payload reset or disabling/cycling of the payload power. The watchdog settings, including enable/disable, can be changed by payload software (setup menu). Time-out values can be selected from as short as seconds to as long as minutes.

The IPMC is supervised by a separate hardware Watchdog, which can not be disabled. IPMC FW retriggers the Watchdog timer.

The IPMC monitors the Port 80 POST codes generated by the payload CPU. The IPMC is connected to various sensors on the Blade that provide temperature sensor readings at all major devices and voltage sensor readings of all major voltages. The IPMC monitors reset events caused by devices like Watchdog, IPMI command, and reset button.

The FRU information of the various modules including front board, RTM, and other modules can be read via the IPMC and if necessary upgraded through the IPMC.

The IPMC features Serial over LAN (SOL) for the payload CPU serial console. The SOL interface is available via the ATCA Base I/F. SOL is activated by specific IPMI commands.

5.9 Serial Redirection

The CPU serial redirection reroutes the console input and output; that is the text output to the text screen and input from the standard keyboard. Typically, the console is used by the BIOS setup menus, BIOS initialization and boot routines, OS boot loaders and loaded OS.

The serial console of the payload CPU is available via SOL. In addition to the SOL capability, the serial console is also available on the blade faceplate using a RJ45 connector with Cisco pin-out. If a SOL session is established, only the output is available on the faceplate. Input is not possible during this time via the faceplate. Alternatively to the CPU serial console, the IPMC serial console is also available on the faceplate serial connector. It can be selected via specific IPMI OEM command.

5.10 Real Time Clock

An external 32.768 kHz crystal sources the internal real time clock inside C604 chipset with a frequency tolerance of 20 PPM. The RTC is fully DS1287, MC14618, PC87911 and Y2K compliant and provides 256 bytes of backed up CMOS RAM (of which 14 bytes containing the RTC time and date info and RTC configuration). The default power-down backup method uses a Super CAP with a 1 Farad capacity.

5.11 Serial ATA

Intel C604 chipset includes a six port serial ATA controller compliant to SATA 2.0 specification. All ports can support data transfer rate of 3.0Gbps, and two ports (Port0 and Port1) can support SATA 3.0, 6.0Gbps.

5.12 IPMI Over LAN

IPMI messages can be transferred over LAN (Base interface) using the RMCP protocol, as defined in the IPMI v1.5 specification, or using the RMCP+ protocol extension, as defined in the IPMI v2.0 specification. The RMCP/RMCP+ packets are formatted to contain IPMI request and response messages, plus additional messages for discovery and authentication.

The IPMI-over-LAN functionality is supported at a level that allows the Serial-over-LAN feature to be implemented.

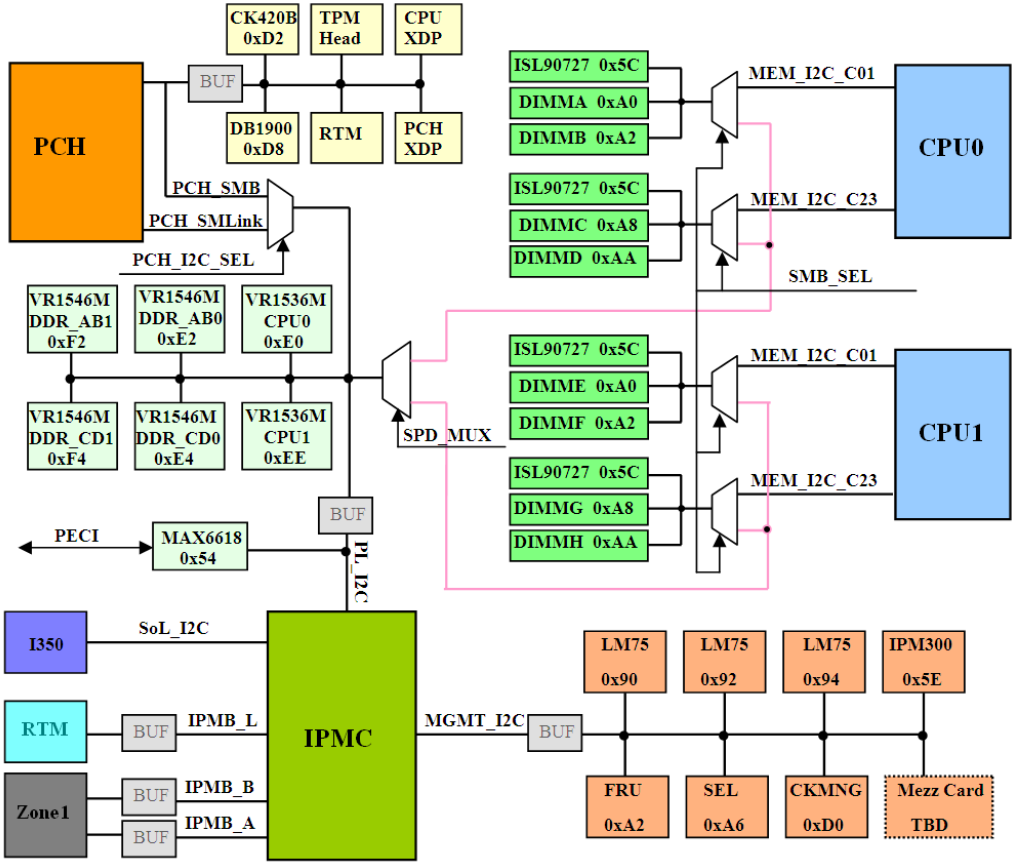
5.13 USB 2.0 Interface

The C604 chipset provides internal USB1.1/ USB 2.0 host controllers with up to 14 USB2.0 ports. Two ports are routed to the faceplate, one port is routed to the RTM on ATCA-7370. The ports available at the faceplate are routed to a dual stacked connector. The ports are USB 2.0 compliant.

5.14 SMBus Connections

The following figure shows the overall SMBus connections on ATCA-7370.

Figure 5-4 Overall SMBus Connections



Note: On the single processor variant the processor and its DIMM sockets are populated on the upper side of the board. Components associated with the second processor are not populated on this product variant.

The IPMC can access the thermal information of DIMM SPD. At beginning of boot, CPU dedicated memory I2C bus owns the DIMM SPD for memory parameter reading. IPMC can access the DIMM SPD for DIMM thermal information through mux control signal.

5.15 Glue Logic FPGA

The Glue Logic FPGA is a programmable logic device used for:

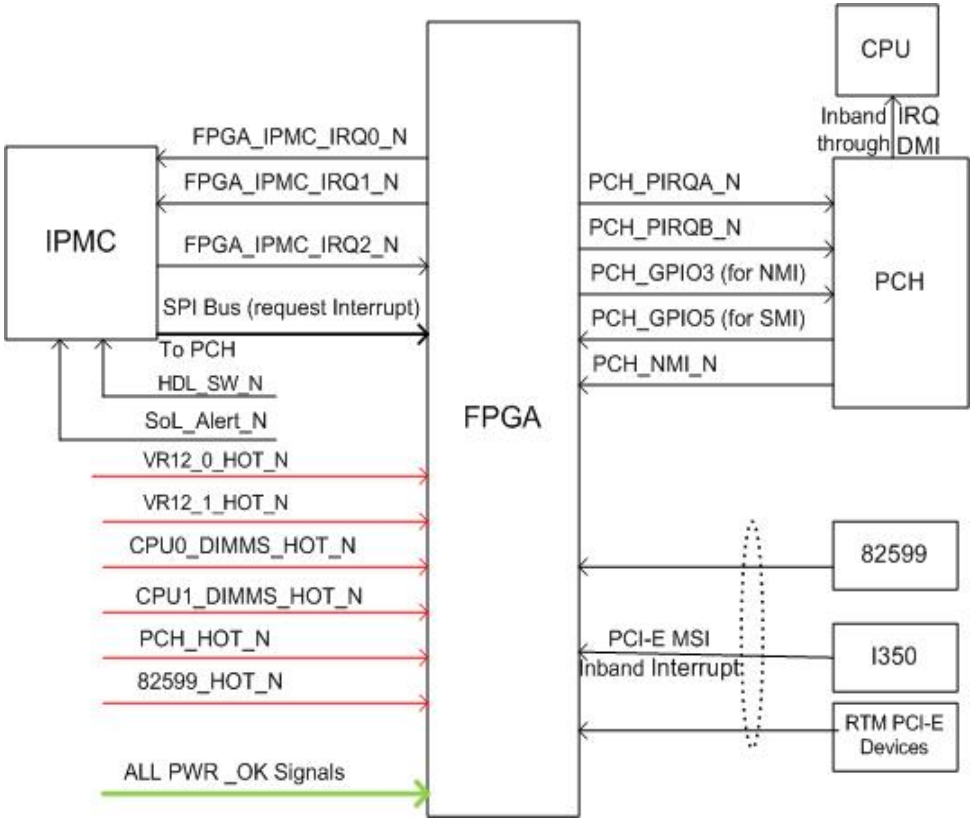
- Power sequence control
- LPC interface under PCH for internal register access
- SPI Interface under IPMC for internal register and BIOS access
- Reset control logic
- Interruption control logic
- BIOS bank selection control
- Dual UART controller with routing control

6.1 Interrupt Structure

The ATCA-7370 supports NON-APIC (legacy PIC Mode) and APIC mode of Interrupt delivery to the CPUs. The 8259 PIC mode interrupt concentrator supports 16 interrupts (8 external signal inputs). The IO-APIC device supports 24 interrupt sources. In APIC mode the C604 chipset supports only Front side bus interrupt delivery (not the serial APIC mode). The following figure and tables summarize the interrupt sources and mappings for ATCA-7370. APIC mode is configured through BIOS after boot-up phase which is done in legacy PIC mode.

The following diagram shows the interrupt signals connection and possible interrupt resources.

Figure 6-1 Interrupt Structure on ATCA-7370



The following table list interrupt resources.

Table 6-1 Interrupt Source Signals List

Source	Signal	Description
IPMC	NMI_N	This is a FPGA register bit written by IPMC through SPI bus to request a NMI interrupt to PCH. this register bit can connect to GPIO3 of PCH to cause a PCH NMI interrupt.
Thermal event	VR12_0_HOT_N VR12_1_HOT_N CPU0_DIMMS_HOT_N	These thermal signals description please refer to chapter 15: Thermal Management. These thermal can be arranged into FPGA register. And when one signal is assert and isn't masked, it can cause a interrupt to IPMC or PCH. this feature can be reserved, and some devices thermal management maybe be through acquire mode to read its thermal information, such as LM75.
Handle switch	HDL_SW	This signal route to IPMC interrupt to process board insertion or removing event.
SoL I2C	SoL_ALERT_N	SoL message interrupt to IPMC
PCIE devices	MSI	PCIE endpoint Devices such as 82599, I350 use MSI in-band interrupt mode.

6.1.1 PIC (Non-APIC) D31:F0 Interrupt Mapping

Table 6-2 Non-APIC (PIC mode/8259 Mode) Interrupt Mapping

	8259 IRQ	Typical Interrupt Source	Interrupt Source
Master	0	Internal	8254 Counter 0, Timer 0 (HPET)
	1	Keyboard	IRQ1 via SERIRQ
	2	Internal	Slave 8259 INTR output
	3	Serial Port A	IRQ3 via SERIRQ, PIRQ#
	4	Serial Port B	IRQ4 via SERIRQ, PIRQ#
	5	Parallel/Generic	IRQ5 via SERIRQ, PIRQ#
	6	Floppy	IRQ6 via SERIRQ, PIRQ#
	7	Parallel/Generic	IRQ7 via SERIRQ, PIRQ#
Slave	8	Internal RTC	Internal RTC, Timer 1 (HPET)
	9	Generic	IRQ9 via SERIRQ, SCI, TCO, or PIRQ#
	10	Generic	IRQ10 via SERIRQ, SCI, TCO, or PIRQ#
	11	Generic	IRQ11 via SERIRQ, SCI, TCO, or PIRQ# or Timer#2 (HPET)
	12	PS/2 Mouse	IRQ12 via SERIRQ, SCI, TCO, or PIRQ# or Timer#3 (HPET)
	13	Internal	State Machine output based on processor FERR# assertion. May optionally be used for SCI or TCO interrupt if FERR# not needed.

Table 6-2 Non-APIC (PIC mode/8259 Mode) Interrupt Mapping

	8259 IRQ	Typical Interrupt Source	Interrupt Source
	14	SATA	SATA Primary (legacy mode), or via SERIRQ or PIRQ#
	15	SATA	SATA Secondary (legacy mode), or via SERIRQ or PIRQ#

IRQ0, 1, 2, 8 and 13 must not be used for PCI interrupts (external inputs PIRQ [A...H]#, which are only reserved for future usage) routing. If an interrupt is used for PCI IRQ [A:H], SCI or TCO it must not be used for ISA (legacy)-style interrupts (via SERIRQ). In PIC Mode (8259.mode), PCI interrupts are mapped to IRQ3-7,9-12, 14 or 15. If IRQ11 is used for Timer 2, software must ensure IRQ11 is not shared with any other devices to guarantee the proper operation of Timer 2. The chipset does not prevent the sharing of IRQ11. Interrupts can individually be programmed to be edge or level, except for IRQ0, IRQ2, IRQ8#, and IRQ13.

6.1.2 APIC (D31:F0) Interrupt Mapping

Table 6-3 APIC Mode Interrupt Mapping

IRQ	Interrupt Source	Notes
0	Cascade from 8259 1	
1		
2	8254 Counter 0, Timer 0 (legacy mode)	
3		
4		
5		
6		
7		
8	RTC, Timer 1 (legacy mode)	

Table 6-3 APIC Mode Interrupt Mapping (continued)

IRQ	Interrupt Source	Notes
9	Option for TCI, TCO	
10	Option for TCI, TCO	
11	Timer 2, Option for TCI, TCO	
12	Timer 3	
13	FERR# logic	
14	SATA Primary (legacy mode)	
15	SATA Secondary (legacy mode)	
16	PIRQ[A]#	For other internal devices see the chipset documentation.
17	PIRQ[B]#	
18	PIRQ[C]#	
19	PIRQ[D]#	
20	PIRQ[E]# (GPIO)	Option for SCI, TCO, and HPET (Timer). For other internal devices see the chipset documentation.
21	PIRQ[F]# (GPIO)	
22	PIRQ[G]# (GPIO)	
23	PIRQ[H]# (GPIO)	

In APIC mode, the PCI Interrupts A:H are mapped to IRQ[16:23].

When programming the polarity of internal interrupt sources on the APIC, interrupts 0 through 15 receive active-high internal interrupt sources; interrupts 16 through 23 receive active-low internal interrupt sources.

6.1.3 Non-Maskable Interrupt Generation

Non-Maskable Interrupt (NMI) is used to force a non-Maskable interrupt to the processor. The processor detects an NMI when it detects a rising edge on NMI. NMI is reset by setting the corresponding NMI source enable/disable bit in the NMI Status and Control register (I/O Register 61h).

The chipset can generate NMI by several sources which are described in following table.

Table 6-4 NMI Sources

Cause of NMI	Comment
SERR# goes active (either internally, externally using SERR# signal, or using message from processor)	Can instead be routed to generate an SCI through the NSI2SCI_EN bit (Device 31: Function 0, TCO Base + 08h, Bit 11).
IOCHK# goes active using SERIRQ# stream (ISA System Error)	Can instead be routed to generate an SCI through the NMI2SCI_EN bit (Device 31: Function 0, TCO Base + 08h, Bit 11).
SECSTS Register Device 31: Function F0 Offset 1Eh, Bit 8.	This is enabled by the Parity Error Response Bit (PER) at Device 30: Function 0 Offset 04, Bit 6.
DEV_STS Register Device 31: Function F0 Offset 06h, Bit 8	
GPIO[15:0] When configured as a General Purpose input and routed as NMI (by GPIO_ROUT at Device 31: Function 0 Offset B8)	

The GPIO[15:0] can generate NMI. On the ATCA-7370, the GPIO3 of PCH connects to the FPGA. The IPMC can request an NMI interrupt through controlling the GPIO3 of PCH connect to FPGA.

The chipset has NMI Status and Control Register and the NMI Enable Register. Both can be used to configure the relevant settings and get the status report. Software can also set NMI2SMI_EN bit in TC01 Control Register to force all NMIs to instead cause SMI. The functionality of this bit is dependent upon the settings of the NMI_EN bit and the GBL_SMI_EN bit, as detailed in the succeeding table.

NMI_EN	GBL_SMI_EN	Description
0b	0b	No SMI# at all because GBL_SMI_EN = 0
0b	1b	SMI# will be caused due to NMI events
1b	0b	No SMI# at all because GBL_SMI_EN = 0
1b	1b	No SMI# due to NMI because NMI_EN = 1

IPMC can initiate a NMI request to processor to cause a warm-reset when the Payload-Watchdog in IPMC is timeout or when IPMC receives a command from shelf-manager.

In Intel Xeon E5-2648L Processor, either SMI or NMI interrupts can be enabled in MC_SMI_CNTRL register. The type of interrupt trigger is based on the following conditions or scenarios:

- A DIMM error counter exceeds the threshold
- Redundancy is lost on a mirrored configuration or
- A sparing operation completes.
- Warm reset request.

This register is set by hardware once operation is complete. Bit is cleared by hardware when a new operation is enabled. An SMI is generated when this bit is set due to a sparing copy completion event.

Following table defines how to determine the cause of an interrupt in the processor.

Table 6-5 Causes of Interrupt

Condition	Cause	Recommended Platform Software Response
MC_SMI_DIMM_ERROR_STATUS. DIMM_ERROR_OVERFLOW_STATUS !=0	The register has one bit for each DIMM error counter that exceeds threshold. This can happen at the same time as any of the other SMI events (Sparring complete, redundancy lost in Mirror Mode)	Examine the associated MC_COR_ECC_CNT_X register. Determine the time since the counter has been cleared. If a spare channel exists, and the threshold has been exceeded faster than would expected given the background rate of correctable errors, sparing should be initiated. The counter should be cleared to reset the overflow bit.
MC_RAS_STATUS.REDUNDANCY_LOSS = 1	One channel of a mirrored pair had an uncorrectable error has been lost.	Raise an indication that a reboot should be scheduled, possibly replace the failed DIMM specified in the MC_SMI_DIMM_ERROR_STATUS register.
MC_SSRSTATUS. CMPLT = 1	A sparring copy operation set up by software has completed.	Advance to the next step in the sparing flow.

6.2 Registers

For register description, the convention shown in Table 6-7 "Register Access Type" and Table 6-7 "Register Access Type" are used.

Table 6-6 Register Default

Default	Description
-	Not applicable or undefined
0 or 1	Default value after RST_N is valid or after PCH_PLTRST deassertion.
Undef.	Undefined value

Table 6-6 Register Default (continued)

Default	Description
<reset>: 0 or 1	Default value after deassertion of the reset signal <reset>.
Ext.	External Reset Source. Default depends on external logic level.

Table 6-7 Register Access Type

Access	Description
r	Read only
w	Write only
r/w	Read and write
w1c	Write-1-to-clear, ignore bit while reading
r/w1c	Read and write-1-to-clear, write 0 has no effect
r/w1s	Read and write-1-to-set, write 0 has no effect
r/w1t	Read and write-1-to-toggle, write 0 has no effect
LPC:	The prefix "LPC:" signals that the access is restricted to the LPC interface.
E. g.: LPC: r/w means that the register bit is read/writable from the LPC interface	
IPMC:	The prefix "IPMC:" signals that the access is restricted to the IPMC SPI interface.
E. g.: IPMC: r/w means that the register bit is read/writable from IPMC SPI interface	

6.2.1 Register Decoding

The FPGA registers may be accessed from the host or the IPMI. For the host, the LPC bus interface is used. The IPMC uses an SPI interface.

6.2.1.1 LPC Decoding

The LPC bus supports different protocols.

6.2.1.1.1 LPC I/O Decoding

The LPC interface responds to LPC I/O accesses listed in the Table 6-8. All other LPC I/O accesses are ignored.

Table 6-8 LPC I/O Register Map Overview

Base Address	Address Size	Address Range Name	Description
0x4E	2	SIW	Super IO Configuration Registers for Index and Date
0x80	1	POSTCODE	POST Code Register
BASE1	8	COM1	UART1. Serial Port 1 (Logical Device 4). BASE1 address is set up during Super IO Configuration.
BASE2	8	COM2	UART2. Serial Port 2. (Logical Device 4). BASE2 address is set up during Super IO Configuration.
0x600	128	REGISTERS	FPGA Registers

All LPC I/O accesses to the address range REGISTERS are decoded by the LPC core.

6.2.1.1.2 LPC Memory Decoding

The LPC interface never responds to LPC Memory accesses.

6.2.1.1.3 LPC Firmware Decoding

The LPC interface never responds to LPC Firmware accesses.

6.2.1.2 SPI Register Decoding

All SPI accesses from the IPMC towards the FPGA with the SPI select signal BMC_SPI_S0_N asserted are for the internal registers.

Table 6-9 IPMC SPI Register

SPI Address Range	Address Range Name	Description
0x00 - 0x7F	REGISTERS	FPGA Registers

6.2.2 POST Code Register

The FPGA provides and 8-bit wide register to store POST codes to the LPC I/O address 0x80.

The IPMC may read the POST code using the SPI interface (with the signal BMC_SPI_S0_N asserted) and the SPI address 0x7F.

Table 6-10 POST Code Register

LPC I/O Address: 0x80			
IPMC SPI Address: 0x7f			
Bit	Description	Default	Access
7:0	POST codes from host	0	LPC: r/w
IPMC: r			

6.2.3 Super IO Configuration Register

After a LPC Reset (ICH_PLTRST_ is asserted) or "Power On Reset" the Super IO is in the Run Mode with the UARTs disabled. They may be configured using the LPC IO Address Range SIW (INDEX and DATA) by placing the Super IO into Configuration Mode. The BIOS uses these configuration addresses to initialize the logical devices at POST. The INDEX and DATA addresses are only valid when the Super IO is in Configuration State. The INDEX and DATA addresses are effective only when the Super IO is in the Configuration State. When the Super IO is not in the Configuration State, reads return 0xFF and write data is ignored.

Table 6-11 Super I/O Configuration Index Register

LPC I/O Address: 0x4E			
Bit	Description	Default	Access
7:0	INDEX. Configuration Index.	0xff	LPC: r/w

Table 6-12 Super I/O Configuration Data Register

LPC I/O Address: 0x4F			
Bit	Description	Default	Access
7:0	DATA Configuration Data.	0xff	LPC: r/w

6.2.3.1 Entering the Configuration State

The device enters the Configuration State by the following contiguous sequence:

1. Write 80H to Configuration Index Port.
2. Write 86H to Configuration Index Port.

6.2.3.2 Exiting the Configuration State

The device exits the configuration state by the following contiguous sequence:

1. Write 68 to Configuration Index Port.
2. Write 08 to Configuration Index Port

6.2.3.3 Configuration Mode

The system sets the logical device information and activates desired logical devices through the INDEX and DATA ports.

The desired configuration registers are accessed in two steps.

1. Write the index of the Logical Device Number Configuration Register (i.e., 07) to the INDEX PORT and then write the number of the desired logical device to the DATA PORT.
2. Write the address of the desired configuration register within the logical device to the INDEX PORT and then write or read the configuration register through the DATA PORT.

- If accessing the Global Configuration Registers, step (1) is not required. The Super IO returns to the RUN State.
- Only two states are defined (Run and Configuration). In the Run State the Super IO is always ready to enter the Configuration State.

6.2.3.4 Super I/O Configuration Registers

Address locations that are not listed are considered reserved register locations. Reads to reserved registers may return non-zero values. Writes to reserved locations may cause system failure.

6.2.3.4.1 Global Control Configuration Registers

The Super IO Global Registers lie in the address range 0x00-0x2F. All eight bits of the ADDRESS Port are used for register selection. All non-implemented registers and bits ignore writes and return zero when read. The INDEX PORT is used to select a configuration register in the chip. The DATA PORT is then used to access the selected register. These registers are accessible only in the Configuration Mode.

Table 6-13 Global Configuration Register Summary

Index Address	Description
0x07	Super IO Logical Device Number
0x20	Super IO Device ID
0x21	Super IO Device Revision

Table 6-13 Global Configuration Register Summary (continued)

Index Address	Description
0x28	Super IO LPC Control
0x29	Super IO SERIRQ and Pre-divide Control

Table 6-14 Super IO Logical Device Number Register

Index Address: 0x07			
Bit	Description	Default	Access
7:0	Logical Device Number: 0x04: Logical Device 4 (UART 1Serial Port 1) 0x05: Logical Device 5 (UART2 Serial Port 2) A write to this register selects the current logical device. This allows access to the control and configuration registers for each logical device.	0	LPC: r/w

Table 6-15 Super IO Device Revision Register

Index Address: 0x21			
Bit	Description	Default	Access
7:0	Device Revision	0x01	LPC: r

Table 6-16 Super IO LPC Control Register

Index Address: 0x28			
Bit	Description	Default	Access
0	LPC Bus Wait States: 1: Long wait states (sync 6)	1	LPC: r
7:1	Reserved	0	LPC: r

Table 6-17 Global Super IO SERIRQ and Pre-divide Control Register

Index Address: 0x29			
Bit	Description	Default	Access
0	SERIRQ enable: 0: disabled. Serial interrupts disabled. 1: enabled. Logical devices participate in interrupt generations.	0	LPC: r/w
1	SERIRQ Mode: 1: Continuous Mode	1	LPC: r
3:2	UART Clock pre-divide 00: divide by 1 01: divide by 8 10: divide by 26 (CLK_UART is 48 MHz) 11: reserved	0	LPC: r/w
7:4	Reserved	0	LPC: r

6.2.3.4.2 Logical Device Configuration Registers

Use to access the registers that are assigned to each logical unit. The Super IO supports two logical units and has two sets of logical device registers. The two logical devices are UART1 (Logical Number 4) and UART2 (Logical Number 5). A separate set (bank) of control and configuration registers exists for each logical device and is selected with the Logical Device Number Register. The INDEX PORT is used to select a specific logical device register. These registers are then accessed through the DATA PORT. The Logical Device registers are accessible only when the device is in the Configuration state.

Table 6-18 Logical Device Configuration Register Summary

Index Address	Description
0x30	Enable
0x60	Base IO Address MSB
0x61	Base IO Address LSB
0x70	Primary Interrupt Select
0x74	Reserved

Table 6-18 Logical Device Configuration Register Summary (continued)

Index Address	Description
0x75	Reserved
0xF0	Reserved

The logical register addresses are shown in the tables below.

Table 6-19 Logical Device Enable Register

Index Address: 0x30			
Bit	Description	Default	Access
0	Logical Device Enable: 0: disabled. Currently selected device is inactive. 1: enabled. . The currently selected device is enabled.	1	LPC: r/w
7:1	Reserved	0	LPC: r

Table 6-20 Logical Device Base IO Address MSB Register

Index Address: 0x60			
Bit	Description	Default	Access
7:0	Logical Device Base IO Address MSB	0	LPC: r/w

Table 6-21 Logical Device Base IO Address LSB Register

Index Address: 0x61			
Bit	Description	Default	Access
2:0	Bits 0 to 2 are read only. Decode is on 8 Byte boundary.	0	LPC: r
7:3	Logical Device Base IO Address LSB. (Bits 3 to 7)	0	LPC: r/w

Registers 0x60 (MSB) and 0x61 (LSB) set the Logical Device Base IO for this logical device. For example for Base IO address 0x3F8 the content of Register 0x60 is 0x03 and the content of Register 0x61is 0xF8.

See table below for Common Decode Ranges:

Table 6-22 Logical Device Common Decode Ranges

IO Address range	Description
0x3F8 - 0x3FF	COM1
0x2F8 - 0x2FF	COM2
0x2E8 - 0x2EF	COM3
0x3E8 - 0x3EF	COM4

Table 6-23 Logical Device Primary Interrupt Register

Index Address: 0x70			
Bit	Description	Default	Access
3:0	Interrupt level is used for Primary Interrupt: 0x0: no interrupt selected 0x1: IRQ1 0x2: IRQ2 0x3: IRQ3 0x4: IRQ4 0x5: IRQ5 0x6: IRQ6 0x7: IRQ7 0x8: IRQ8 0x9: IRQ9 0xA: IRQ10 0xB: IRQ11 0xC: IRQ12 0xD: IRQ13 0xE: IRQ14 0xF: IRQ15	0	LPC: r/w

Table 6-23 Logical Device Primary Interrupt Register (continued)

Index Address: 0x70			
Bit	Description	Default	Access
7:4	Reserved	0	LPC: r

An Interrupt is activated by enabling this device (offset 0x30), setting this register to a non-zero value and setting any combination of bits 0-4 in the corresponding UART IER and the occurrence of the corresponding UART event (i.e. Modem Status Change, Receiver Line Error Condition, Transmit Data Request, Receiver Data Available or Receiver Time Out) and setting the OUT2 bit in the MCR.

Table 6-24 Logical Device 0x74 Reserved Register

Index Address: 0x74			
Bit	Description	Default	Access
7:0	Reserved	0x04	LPC: r

Table 6-25 Logical Device 0x75 Reserved Register

Index Address: 0x75			
Bit	Description	Default	Access
7:0	Reserved	0x04	LPC: r

Table 6-26 Logical Device 0xF0 Reserved Register

Index Address: 0xF0			
Bit	Description	Default	Access
7:0	Reserved	0	LPC: r

6.2.4 UART1 and UART2 Register Map

6.2.4.1 UART Register Overview

Table 6-1 "Interrupt Source Signals List" shows the registers and their addresses as offsets of a base address for one or two UART.

The most significant bit of the Serial Line Control Register (SCR) is the Divisor Latch Bit (DLAB). Its state effects the selection of certain UART registers. The DLAB bit must be set high by the system software to access the Baud Rate Generator Divisor Latches (DLL and DLM)

Table 6-27 UART Register Overview

LPC IO Address	DLAB Bit value	Description
Base	0	Receiver Buffer (RBR). Read Only
Base	0	Transmitter Holding (THR). Write Only.
Base + 1	0	Interrupt Enable Register (IER)
Base + 2	X	Interrupt Identification Register (IIR). Read Only
Base + 2	X	FIFO Control Register (FCR). Write Only.
Base + 3	X	Line Control Register (LCR)
Base + 4	X	Modem Control Register (MCR)
Base + 5	X	Line Status Register (LSR). Read Only
Base + 6	X	Modem Status Register (MSR). Read Only
Base + 7	X	Scratch Pad Register (SCR).
Base	1	Divisor Latch LSB (DLL)
Base + 1	1	Divisor Latch MSB (DLM)

6.2.5 UART Registers DLAB=0

6.2.5.1 Receiver Buffer Register

In non-FIFO mode, the Receiver Buffer Register (RBR) holds the character received by the UART's Receive Shift Register. If less than 8-bits are received, the bits are right-justified and the leading bits are zeroed. Reading the register empties the register and resets the data ready (DR) bit in the line status register to zero. Other bits, errors or otherwise, are not cleared. In FIFO mode, this register latches the value of the data byte at the top of the FIFO.

Table 6-28 Receiver Buffer Register (RBR) if DLAB=0

LPC IO Address: Base			
Bit	Description	Default	Access
7:0	Receiver Buffer register (RBR)	Undef.	LPC: r

6.2.5.2 Transmitter Holding Register (THR)

This register holds the next data byte to be transmitted. When the transmit shift register becomes empty, the contents of the THR is loaded into the shift register. The transmit data request (TDRQ) bit in the line status register is set to one.

Table 6-29 Transmitter Holding Register (THR) if DLAB=0

LPC IO Address: Base			
Bit	Description	Default	Access
7:0	Transmitter Holding register (THR)	Undef.	LPC: w

Writing to THR while in FIFO mode puts THR to the top. The data at the bottom of the FIFO is loaded to the shift register when it is empty.

6.2.5.3 Interrupt Enable Register (IER)

This register enables four types of interrupts which independently activate the int signal and sets a value in the Interrupt Identification Register. Each of the four interrupt types can be disabled by resetting the appropriate bit of the IER register. Similarly, by setting the appropriate bits, selected interrupts can be enabled.

Table 6-30 Interrupt Enable Register (IER), if DLAB=0

LPC IO Address: Base + 1			
Bit	Description	Default	Access
0	Receive data interrupt enable/disable: 1: receive data interrupt enabled 0: receive data interrupt disabled	0	LPC: r/w
1	Transmitter holding register empty (THRE) interrupt enable/disable 1: THRE interrupt enabled 0: THRE interrupt disabled	0	LPC: r/w
2	Receiver line status interrupt enable/disable 1: receiver line status interrupt enabled 0: receiver line status interrupt disabled	0	LPC: r/w
3	Modem status interrupt enable/disable: 1: modem status interrupt enabled 0: modem status interrupt disabled	0	LPC :r/w
7:4	Reserved	0	LPC: r

6.2.5.4 Interrupt Identification Register (IIIR)

In order to minimize software overhead during data character transfers, UART prioritizes interrupts into four levels and records these in the IIIR. The IIIR stores information indicating that a prioritized interrupt is pending, as well as the source of that interrupt. The four levels are listed in the succeeding table.

Table 6-31 UART Interrupt Priorities2

Priority Level	Interrupt Source
1 (highest)	Receiver Line Status. One or more error bits were set.
2	Received Data is available. In FIFO mode, trigger level was reached; in non-FIFO mode, RBR has data.
2	Receiver Time out occurred. It happens in FIFO mode only, when there is data in the receive FIFO but no activity for a time period.
3	Transmitter requests data. In FIFO mode, the transmit FIFO is half or more than half empty; in non-FIFO mode, THR is read already
4	Modem Status: one or more of the modem input signals has changed state

Table 6-32 Interrupt Identification Register (IIIR)

LPC IO Address: Base + 2			
Bit	Description	Default	Access
0	Interrupt status bit: 1: no interrupt pending 0: interrupt pending	1	LPC: r
2:1	Interrupt priority level and source: 11: Receiver line status 10: Receiver data available 01: Transmitter holding register empty 00: Modem status	0	LPC: r
3	Time Out Detected: 0: No time out interrupt is pending 1: Character time-out indication (FIFO mode only)	0	LPC: r

Table 6-32 Interrupt Identification Register (IIIR)

LPC IO Address: Base + 2			
Bit	Description	Default	Access
5:4	Reserved	0	LPC: r
7:6	FIFO Mode Enable bits: 00: Default mode 01: Reserved 10: Reserved 11: FIFO mode	0	LPC: r

Table 6-33 Interrupt Identification Register Decode

Interrupt ID	Interrupt Set/Reset Function			
3:0	Priority	Type	Source	Reset Control
0b0001	-	None	No Interrupt is pending	-
0b0110	1	Receiver Line Status	Overrun Error, Parity Error, Framing Error, Break Interrupt.	Reading the Line Status Register.
0b0100	2	Received Data Available.	Non-FIFO mode: Receive Buffer is full.	Non-FIFO mode: Reading the Receiver Buffer Register.
			FIFO mode: Trigger level was reached.	FIFO mode: Reading bytes until Receiver FIFO drops below trigger level or setting RESETRF bit in FCR register.
0b1100		Character Timeout indication.	FIFO Mode only: At least 1 character is in receiver FIFO and there was no activity for a time period.	Reading the Receiver FIFO or setting RESETRF bit in FCR register
0b0010	3	Transmit FIFO Data Request	Non-FIFO mode: Transmit Holding Register Empty	Reading the IIR Register (if the source of the interrupt) or writing into the Transmit Holding Register.

Table 6-33 Interrupt Identification Register Decode (continued)

Interrupt ID	Interrupt Set/Reset Function			
3:0	Priority	Type	Source	Reset Control
			FIFO mode: Transmit FIFO has half or less than half data.	Reading the IIR Register (if the source of the interrupt) or writing to the Transmitter FIFO.
0b0000	4	Modem Status	Clear to Send, Data Set Ready, Ring Indicator, Received Line Signal Detect	Reading the modem status register

6.2.5.5 FIFO Control Register (FCR)

FCR is a write-only register that is located at the same address as the IIR (IIR is a read-only register). FCR enables/disables the transmitter/receiver FIFOs, clears the transmitter/receiver FIFOs, and sets the receiver FIFO trigger level.

Table 6-34 FIFO Control Register (FCR)

LPC IO Address: Base + 2			
Bit	Description	Default	Access
0	FIFO enable/disable: 1: Transmitter and Receiver FIFO enabled 0: FIFO disabled	0	LPC: w
1	Receiver FIFO reset: 1: Bytes in receiver FIFO and counter are reset. Shift register is not reset (bit is self-clearing) 0: No effect	0	LPC: w
2	Transmit FIFO reset: 1: Bytes in receiver FIFO and counter are reset. Shift register is not reset (bit is self-clearing) 0: No effect	0	LPC: w
3	Receiver/Transmitter ready. Not supported.	0	LPC: w

Table 6-34 FIFO Control Register (FCR) (continued)

LPC IO Address: Base + 2			
Bit	Description	Default	Access
5:4	Reserved	0	LPC: w
7:6	Receiver FIFO interrupt trigger level: 00: 1 byte 01: 4 bytes 10: 8 bytes 11: 14 bytes	0	LPC: w

6.2.5.6 Line Control Register (LCR)

The system programmer of the LCR specifies the format of the asynchronous data communications exchange. The serial data format consists of a start bit (logic 0), five to eight data bits, an optional parity bit, and one or two stop bits (logic 1). The LCR has bits for accessing the Divisor Latch and causing a break condition. The programmer can also read the contents of the Line Control Register. The read capability simplifies system programming and eliminates the need for separate storage in system memory.

Table 6-35 Line Control Register (LCR)

LPC IO Address: Base + 3			
Bit	Description	Default	Access
1:0	Serial character WORD length: 00: 5 bits 01: 6 bits 10: 7 bits 11: 8 bits	0	LPC: r/w
2	Stop bit length: 1: 1.5 stop bits for 5 bit WORD length 1: 2 stop bits for 6, 7, and 8 bit WORD length 0: 1 stop bit for any serial character WORD length	0	LPC: r/w

Table 6-35 Line Control Register (LCR) (continued)

LPC IO Address: Base + 3			
Bit	Description	Default	Access
3	Parity enable/disable When bit 3 is set, a parity bit is generated in transmitted data between the last data WORD bit and the first stop bit. In received data, if bit 3 is set, parity is checked. When bit 3 is cleared, no parity is generated or checked.: 1: Parity enabled 0: Parity disabled	0	LPC: r/w
4	Parity even/odd When parity is enabled and bit 4 is set, even parity (an even number of logic ones in the data and parity bits) is selected. When parity is disabled and bit 4 is cleared, odd parity (an odd number of logic ones) is selected.: 1: Even parity 0: Odd parity	0	LPC: r/w
5	Stick parity When bits 3, 4, and 5 are set, the parity bit is transmitted and checked as cleared. When bits 3 and 5 are set and bit 4 is cleared, the parity bit is transmitted and checked as set. If bit 5 is cleared, stick parity is disabled.: 1: Stick parity enabled 0: Stick parity disabled	0	LPC: r/w
6	Break control bit Bit 6 is set to force a break condition, i.e. a condition where TXD is forced to the spacing (cleared) state. When bit 6 is cleared, the break condition is disabled and has no affect on the transmitter logic. It only effects TXD: 1: Break condition enabled 0: Break condition disabled	0	LPC: r/w

Table 6-35 Line Control Register (LCR) (continued)

LPC IO Address: Base + 3			
Bit	Description	Default	Access
7	Divisor latch access bit (DLAB) Bit 7 must be set to access the divisor latches of the baud generator during a read or write. Bit 7 must be cleared during a read or write to access the RBR, THR, or IER.: 1: Access to DLL and DLM registers 0: Access to RBR, THR and IER registers	0	LPC: r/w

6.2.5.7 Modem Control Register (MCR)

The MCR is an 8-bit register that controls the interface with the modem or data set (or any peripheral device emulating a modem).

Table 6-36 Modem Control Register (MCR)

LPC IO Address: Base + 4			
Bit	Description	Default	Access
0	Data terminal ready (DTR#) output control:		
	1: DTR# output in low (active) state		
	0: DTR# output in high state	0	LPC: r/w
1	Request to send (RTS#) output control: 1: RTS# output in low (active) state 0: RTS# output in high state	0	LPC: r/w
2	User output control signal (OUT1#): 1: OUT1# output in high state 0: OUT1# output in low state Not supported	0	LPC: r/w
3	User output control signal (OUT2#): 1: OUT2# output in high state 0: OUT2# output in low state Not supported	0	LPC: r/w

Table 6-36 Modem Control Register (MCR) (continued)

LPC IO Address: Base + 4			
Bit	Description	Default	Access
4	Local loop back diagnostic control When loop back is activated: Transmitter TXD is set high. Receiver RXD is disconnected. Output of Transmitter Shift register is looped back into the receiver shift register input. Modem control inputs are disconnected Modem control outputs are internally connected to modem control inputs. Modem control outputs are forced to the inactive (high) levels: 1: Loop back mode activated 0: Normal operation	0	LPC: r/w
5	Autoflow control enable (AFE): 1: Autoflow control enabled (auto-RTS# and auto-CTS# or auto-CTS# only enabled) 0: Autoflow control disabled	0	LPC: r/w
7:6	Reserved	0	LPC: r

6.2.5.8 Line Status Register (LSR)

This register provides status information to the processor concerning the data transfers. Bits 5 and 6 show information about the transmitter section. The rest of the bits contain information about the receiver.

In non-FIFO mode, three of the LSR register bits, parity error, framing error, and break interrupt, show the error status of the character that has just been received. In FIFO mode, these three bits of status are stored with each received character in the FIFO. LSR shows the status bits of the character at the top of the FIFO. When the character at the top of the FIFO has errors, the LSR error bits are set and are not cleared until software reads LSR, even if the character in the FIFO is read and a new character is now at the top of the FIFO.

Bits one through four are the error conditions that produce a receiver line status interrupt when any of the corresponding conditions are detected and the interrupt is enabled. These bits are not cleared by reading the erroneous byte from the FIFO or receive buffer.

They are cleared only by reading LSR. In FIFO mode, the line status interrupt occurs only when the erroneous byte is at the top of the FIFO. If the erroneous byte being received is not at the top of the FIFO, an interrupt is generated only after the previous bytes are read and the erroneous byte is moved to the top of the FIFO.

Table 6-37 Line Status Register (LSR)

LPC IO Address: Base + 5			
Bit	Description	Default	Access
0	Receiver data ready (DR) indicator DR is set whenever a complete incoming character has been received and transferred into the RBR or the FIFO. DR is cleared by reading all of the data in the RBR or the FIFO: 1: New data received 0: No new data	0	LPC: r
1	Overrun error (OE) indicator When OE is set, it indicates that before the character in the RBR was read, it was overwritten by the next character transferred into the register. OE is cleared every time the CPU reads the contents of the LSR. If the FIFO mode data continues to fill the FIFO beyond the trigger level, an overrun error occurs only after the FIFO is full and the next character has been completely received in the shift register. An overrun error is indicated to the CPU as soon as it happens. The character in the shift register is overwritten but it is not transferred to the FIFO: 1: Overrun error occurred 0: No overrun error	0	LPC: r

Table 6-37 Line Status Register (LSR) (continued)

LPC IO Address: Base + 5			
Bit	Description	Default	Access
2	Parity Error (PE) indicator When PE is set, it indicates that the parity of the received data character does not match the parity selected in the LCR (bit 4). PE is cleared every time the CPU reads the contents of the LSR. In the FIFO mode, this error is associated with the particular character in the FIFO to which it applies. This error is revealed to the CPU when its associated character is at the top of the FIFO: 1: Parity error occurred 0: No parity error	0	LPC: r
3	Framing Error (FE) indicator When FE is set, it indicates that the received character did not have a valid (set) stop bit. FE is cleared every time the CPU reads the contents of the LSR. In the FIFO mode, this error is associated with the particular character in the FIFO to which it applies. This error is revealed to the CPU when its associated character is at the top of the FIFO. The ACE tries to resynchronize after a framing error. To accomplish this, it is assumed that the framing error is due to the next start bit. The ACE samples this start bit twice and then accepts the input data: 1: Framing error occurred 0: No framing error	0	LPC: r

Table 6-37 Line Status Register (LSR) (continued)

LPC IO Address: Base + 5			
Bit	Description	Default	Access
4	Break Interrupt (BI) indicator When BI is set, it indicates that the received data input was held low for longer than a full-word transmission time. A full-word transmission time is defined as the total time to transmit the start, data, parity, and stop bits. BI is cleared every time the CPU reads the contents of the LSR. In the FIFO mode, this error is associated with the particular character in the FIFO to which it applies. This error is revealed to the CPU when its associated character is at the top of the FIFO. When a break occurs, only one 0 character is loaded into the FIFO. The next character transfer is enabled after RXD goes to the marking state for at least two Receiver CLK samples and then receives the next valid start bit: 1: Full WORD transmission time exceeded 0: Normal operation	0	LPC: r
5	Transmit Holding Register Empty (THRE) indicator THRE is set when the THR is empty, indicating that the ACE is ready to accept a new character. If the THRE interrupt is enabled when THRE is set, an interrupt is generated. THRE is set when the contents of the THR are transferred to the TSR. THRE is cleared concurrent with the loading of the THR by the CPU. In the FIFO mode, THRE is set when the transmit FIFO is empty; it is cleared when at least one byte is written to the transmit FIFO: 1: THR/Transmit FIFO empty 0: THR/Transmit FIFO contains data	1	LPC: r

Table 6-37 Line Status Register (LSR) (continued)

LPC IO Address: Base + 5			
Bit	Description	Default	Access
6	Transmitter Empty (TEMT) indicator TEMT bit is set when the THR and the TSR are both empty. When either the THR or the TSR contains a data character, TEMT is cleared. In the FIFO mode, TEMT is set when the transmitter FIFO and shift register are both empty: 1: THR/Transmit FIFO/TSR empty 0: THR/Transmit FIFO/TSR contains data	1	LPC: r
7	FIFO data error In the FIFO mode, LSR7 is set when there is at least one parity, framing, or break error in the FIFO. It is cleared when the microprocessor reads the LSR and there are no subsequent errors in the FIFO. If FIFO is not used, bit always reads 0: 1: FIFO data error encountered 0: No FIFO error encountered	0	LPC: r

6.2.5.9 Modem Status Register (MSR)

The MCR is an 8-bit register that provides the current state of the control lines from the modem or data set (or a peripheral device emulating a modem) to the processor. In addition to this current state information, four bits of the Modem Status register provide change information. Bits 03:00 are set to a logic 1 when a control input from the Modem changes state. They are reset to logic 0 when the processor reads the Modem Status register.

When bits 0, 1, 2, or 3 are set to logic 1, a Modem Status interrupt is generated if bit 3 of the Interrupt Enable Register is set.

Table 6-38 Modem Status Register (MSR)

LPC IO Address: Base + 6			
Bit	Description	Default	Access
0	Change in clear-to-send (DCTS) indicator DCTS indicates that the CTS# input has changed state since the last time it was read by the CPU. When DCTS is set (autoflow control is not enabled and the modem status interrupt is enabled), a modem status interrupt is generated. When autoflow control is enabled (DCTS is cleared), no interrupt is generated: 1: Change in state of CTS# input since last read 0: No change in state of CTS# input since last read	0	LPC: r/w
1	Change in data set ready (DDSR) indicator DDSR indicates that the DSR# input has changed state since the last time it was read by the CPU. When DDSR is set and the modem status interrupt is enabled, a modem status interrupt is generated: 1: Change in state of DSR# input since last read 0: No change in state of DSR# input since last read	0	LPC: r/w
2	Trailing edge of the ring indicator (TERI) detector TERI indicates that the RI# input to the chip has changed from a low to a high level. When TERI is set and the modem status interrupt is enabled, a modem status interrupt is generated. Not supported.	0	LPC: r/w

Table 6-38 Modem Status Register (MSR) (continued)

LPC IO Address: Base + 6			
Bit	Description	Default	Access
3	Change in data carrier detect (DDCD) indicator DDCD indicates that the DCD# input to the chip has changed state since the last time it was read by the CPU. When DDCD is set and the modem status interrupt is enabled, a modem status interrupt is generated. Not supported.	0	LPC: r/w
4	Complement of the clear-to-send (CTS#) input When the Asynchronous Communications Element (ACE) is in diagnostic test mode (LOOP [MCR4] = 1), this bit is equal to the MCR bit 1 (RTS#).	Ext.	LPC: r
5	Complement of the data set ready (DSR#) input When the ACE is in the diagnostic test mode (LOOP [MCR4] = 1), this bit is equal to the MCR bit 0 (DTR#).	Ext.	LPC: r
6	Complement of the ring indicator (RI#) input When the ACE is in the diagnostic test mode (LOOP [MCR4] = 1), this bit is equal to the MCR bit 2 (OUT1#). Not supported.	Ext.	LPC: r
7	Complement of the data carrier detect (DCD#) input When the ACE is in the diagnostic test mode (LOOP [MCR4] = 1), this bit is equal to the MCR bit 3 (OUT2#). Not supported.	Ext.	LPC: r

6.2.5.10 Scratch Register (SCR)

This 8-bit read/write register has no effect on the UART. It is intended as a scratchpad register for use by the programmer.

Table 6-39 Scratch Register (SCR)

LPC IO Address: Base + 7			
Bit	Description	Default	Access
7:0	Scratch Register (SCR) The scratch register is an 8 bit register that is intended for the programmer's use as a scratch pad in the sense that it temporarily holds the programmer's data without affecting any other ACE operation.	Undefined	LPC: r/w

6.2.6 Programmable Baud Rate Generator

The UART contains a programmable Baud Rate Generator that is capable of taking the UART_CLK input and dividing it by any divisor from 1 to (2 16 -1). The output frequency of the Baud Rate Generator is 16 times the baud rate. Two 8-bit latches store the divisor in a 16-bit binary format. These Divisor Latches must be loaded during initialization to ensure proper operation of the Baud Rate Generator. If both Divisor Latches are loaded with 0, the 16X output clock is stopped. Upon loading either of the Divisor latches, a 16-bit baud counter is immediately loaded. This prevents long counts on initial load. Access to the Divisor latch can be done with a word write.

The UART_CLK is the CLK_UART (48MHz) input divided by the pre-divider set by the Super IO Configuration Register (Offset 0x29).

The baud rate of the data shifted in/out of the UART is given by:

Baud Rate = UART_CLK / (16X Divisor)

For example, if the pre-divider is 26 the UART_CLK is 1.8461538MHz. When the divisor is 12, the baud rate is 9600.

A Divisor value of 0 in the Divisor Latch Register is not allowed.

Table 6-40 Divisor Latch LSB Register (DLL), if DLAB=1

LPC IO Address: Base			
Bit	Description	Default	Access
7:0	Divisor Latch LSB (DLL)	Undef.	LPC: r/w

Table 6-41 Divisor Latch MSB Register (DLM), if DLAB=1

LPC IO Address: Base + 1			
Bit	Description	Default	Access
7:0	Divisor Latch MSB (DLM)	Undef.	LPC: r/w

6.3 FPGA Register Mapping

6.3.1 LPC I/O Register Map

The FPGA registers may be accessed via LPC I/O cycles in the I/O address range REGISTERS. See Table 6-42 "FPGA Register Map Overview". For an LPC register access, use the base address 0x600 and add the Address Offset. An LPC I/O write-access to an address not listed in this table or marked with a "-" in the LPC I/O column is ignored. A corresponding read access delivers always zero.

Note: LPC I/O Address = 0x600 + Address Offset

6.3.2 IPMC SPI Register Map

The FPGA registers may be accessed using the IPMC SPI transactions (with the signal BMC_SPI_S0_N asserted). See Table 6-42 "FPGA Register Map Overview". A SPI write-access to an address not listed in this table or marked with a "-" in the IPMC SPI column is ignored. A corresponding read access delivers always zero.

Table 6-42 FPGA Register Map Overview

Address Offset [1]	LPC I/O	IPMC SPI	Description
0x00	r	r	Module Identification Register
0x01	r	r	FPGA Version Register
0x02	-	-	Reserved
0x03	rw	r	Serial Redirection Control Register
0x04	r	rw	Serial over LAN (SOL) Control Register
0x05	r	rw	Serial Routing Register
0x06	r	rw	IPMC Power Level Register
0x07	-	rw	Payload Power Control Register
0x08	rw	rw	I2C Switch Control Register
0x09	-	rw	Payload Power-button Register
0x0A~0E	-	-	Reserved
0x0F	rw	rw	Reset Mask Register
0x10	rw	rw	Reset Function Register
0x11	-	w	IPMC Reset Payload Request Register
0x12	w	-	BIOS Reset Payload Request Register
0x13	w	-	OS Reset Payload Request Register
0x14	-	rw	Payload Reset Source for IPMC Register
0x15	rw	-	Payload Reset Source for BIOS Register
0x16	rw	-	Payload Reset Source for OS Register
0x17	-	rw	IPMC Watchdog Timeout Register

[1] For LPC I/O access, add the LPC I/O Base Address 0x600

Table 6-42 FPGA Register Map Overview (continued)

Address Offset [1]	LPC I/O	IPMC SPI	Description
0x18	rw	-	IPMC Watchdog Timeout for BIOS Register
0x19	rw	-	IPMC Watchdog Timeout for OS Register
0x1A	rw	-	FPGA-Payload-Watchdog Threshold Low-byte Register
0x1B	rw	-	FPGA-Payload-Watchdog Threshold High-byte Register
0x1C	rw	-	FPGA-Payload-Watchdog Clear Register
0x1D~1E	-	-	Reserved
0x1F	-	w	FPGA-IPMC-Watchdog Threshold Register
0x20~2D	-	-	Reserved
0x2E	-	rw	HFI Mode Enable Register
0x2F~32	-	rw	HFI Mode POL Control Registers
0x33~36	-	rw	HFI Mode Reset Control Registers
0x37~3F	-	-	Reserved
0x40	r	rw	Flash Control Register
0x41~48	-	-	Reserved
0x49	r	rw	IPMC Scratch Register 0.
0x4A	r	rw	RTM Status and Control Register
0x4B~55	-	-	Reserved
0x56	r	rw	Blue LED Status and Control Register
0x57	rw	r	User LED Status and Control Register
0x58	r	r	MISC Status and Control Register
0x59	r	r	Debug Switch and LED Status Register
0x5A	r	r	CPU Error Status Register
0x5B	r	rw	Cave Creek Module Status and Control Register
0x5C	r	rw	ACPI Status and Control Register

[1]For LPC I/O access, add the LPC I/O Base Address 0x600

Table 6-42 FPGA Register Map Overview (continued)

Address Offset [1]	LPC I/O	IPMC SPI	Description
0x5D	-	-	Reserved
0x5E~5F	r	rw	Interface Control Registers 0~1
0x60~63	-	rw	PCA9555#0 Registers
0x64~67	-	rw	PCA9555#1 Registers
0x68~6B	-	rw	PCA9555#2 Registers
0x6C~6F	-	rw	PCA9555#3 Registers
0x70~73	-	rw	PCA9555#4 Registers
0x74~75	r	r	Thermal Event Registers 0~1
0x76~7D	rw	r	LPC Scratch Registers 0~7
0x7E	r	rw	IPMC Scratch Register 1.
0x7F	r	r	POST Code Register
[1]For LPC I/O access, add the LPC I/O Base Address 0x600			

6.3.3 Module Identification Register

The Module Identification Registers identifies the ATCA-7370.

Table 6-43 Module Identification Register

Address Offset: 0x00			
Bit	Description	Default	Access
7:0	ATCA-7370 Module Identification	0x70	r

6.3.4 Version Register

The version register provides the version of the FPGA bit stream. The initial value starts at 0x01 and will be incremented with each new release.

Table 6-44 Version Register

Address Offset: 0x01			
Bit	Description	Default	Access
7:0	Specifies FPGA version	-	r

6.3.5 Serial Redirection Console Register

The BIOS sets the corresponding bit, which is used for serial direction. The IPMC uses this information to route the corresponding port serial IPMC interface in case of serial over lan (SOL).

BIOS should never set both status bits.

Table 6-45 Serial Redirection Control Register

Address Offset: 0x03			
Bit	Description	Default	Access
0	COM1 used for serial redirection: 0: COM1 not used for serial redirection 1: COM1 used for serial redirection	0	LPC: r/w IPMC: r
1	COM2 use for serial redirection 0: COM2 not used for serial redirection 1: COM2 used for serial redirection	0	LPC: r/w IPMC: r
7:2	Reserved	0	r

6.3.6 Serial Over LAN (SOL) Control Register

The IPMC software can route the serial data from serial port 1 (COM1) or serial port 2 (COM2) to the IPMC.

When both control bits are enabled, bit 1 is ignored.

Table 6-46 SOL Control Register

Address Offset: 0x04			
Bit	Description	Default	Access
0	SOL over COM1 enable: 0: disabled 1: enabled. COM1 is forwarded to IMPC	0	IPMC: r/w LPC: r
1	SOL over COM2 enable: 0: disabled 1: enabled. COM2 is forwarded to IMPC	0	IPMC: r/w LPC: r
7:2	Reserved	0	r

6.3.7 Serial Routing Register

Table 6-47 Serial Routing Register

Address Offset: 0x05			
Bit	Description	Default	Access
1:0	00: COM1 to Faceplate and COM2 to RTM 01: COM1 to RTM and COM2 to Faceplate 10: BMC to Faceplate and COM2 to RTM 11: BMC to Faceplate and COM1 to RTM	00	IPMC: r/w LPC: r

Table 6-47 Serial Routing Register

Address Offset: 0x05			
Bit	Description	Default	Access
7:2	Reserved	0	r

When bit1 in this register is 0, FPGA_COM_SW outputs high level. When it is in 1, it outputs to low level.

6.3.8 IPMC Power Level Register

Table 6-48 IPMC Power Level Register

Address Offset: 0x06			
Bit	Description	Default	Access
7:0	IPMC Power Level. IPMC writes a value, which represents a defined power level.	0x00	IPMC: r/w LPC: r

Whenever the IPMC writes and data into this register, it should also produce an 8 ms negative pulse on FPGA_PCH_GPIO5 to notify payload.

6.3.9 Payload Power Control Register

Table 6-49 Payload Power Control Register

Address Offset: 0x07			
Bit	Description	Default	Access
0	IPMC turn on payload power request: 1: Payload power on 0: Payload power off	0	IPMC: r/w
7:1	Reserved	0	r

6.3.10 I2C Switch Control Register

Table 6-50 I2C Switch Control Register

Address Offset: 0x08			
Bit	Description	Default	Access
0	FPGA_SPD_MUX_S[0]	0	IPMC: r/w LPC: r
1	FPGA_SPD_MUX_S[1]	1	IPMC: r LPC: r/w
2	FPGA_PCH_I2C_SEL	0	IPMC: r/w LPC: r
7:3	Reserved	0	r

6.3.11 Payload Power-Button Register

Table 6-51 Payload Power-Button Register

Address Offset: 0x09			
Bit	Description	Default	Access
0	FPGA_PCH_PWRBTN_N	1	IPMC: r/w
7:1	Reserved	0	r

6.3.12 Reset Registers

6.3.12.1 Reset Mask Register

The reset mask register enables or disables forwarding of a reset source to reset output signal. Only Push Button Resets requests are affected by the reset mask register. The register default values are latched when RST_N is asserted. This register can be read or written by the host CPU. A one in the register bit indicates that the associated reset is enabled. A zero indicates that the associated reset source is masked.

Table 6-52 Reset Mask Register

Address Offset: 0x0F			
Bit	Description	Default	Access
0	Reserved	0	r
1	Reserved	0	r
2	Enable front board push button reset payload 1: enabled 0: disabled	0	LPC: r/w IPMC: r
3	Enable IPMC reset payload 1: enabled 0: disabled	1	LPC: r IPMC: r/w

Table 6-52 Reset Mask Register (continued)

Address Offset: 0x0F			
Bit	Description	Default	Access
4	Enable RTM push button reset payload 1: enabled 0: disabled	0	LPC: r/w IPMC: r
5	Enable FPGA Watchdog reset payload 1: enabled 0: disabled	0	LPC: r/w IPMC: r
6	Enable BIOS reset payload 1: enabled 0: disabled	0	LPC: r/w IPMC: r
7	Enable OS reset payload 1: enabled 0: disabled	0	LPC: r/w IPMC: r

6.3.12.2 Reset Function Register

The reset function register selects the reset function for a certain reset source among warm-reset and cold-reset. If a cold-reset is on going, a warm-reset request will be ignored.

Table 6-53 Reset Function Register

Address Offset: 0x10			
Bit	Description	Default	Access
0	Reserved	0	r
1	Reserved	0	r
2	Select the function of front board push button payload request 1: Warm-reset 0: Cold-reset	1	LPC: r/w IPMC: r

Table 6-53 Reset Function Register (continued)

Address Offset: 0x10			
Bit	Description	Default	Access
3	Select the function of IPMC reset payload request 1: Warm-reset 0: Cold-reset	0	LPC: r IPMC: r/w
4	Select the function of RTM push button reset payload request 1: Warm-reset 0: Cold-reset	1	LPC: r/w IPMC: r
5	Select the function of FPGA watchdog reset 1: Warm-reset 0: Cold-reset	1	LPC: r/w IPMC: r
6	Select the function of BIOS reset payload request 1: Warm-reset 0: Cold-reset	1	LPC: r/w IPMC: r
7	Select the function of OS reset payload request 1: Warm-reset 0: Cold-reset	1	LPC: r/w IPMC: r

6.3.12.3 IPMC Reset Payload Request Register

IPMC software writes a magic word 0x55 into this address will launch a payload reset request. If related bit in Reset Mask Register is high, a warm or cold reset will occur basing on Reset Function Register bit.

Table 6-54 IPMC Reset Payload Request Register

Address Offset: 0x11			
Bit	Description	Default	Access
7:0	Writing magic word 0x55 will cause a reset request	-	IPMC: w

6.3.12.4 BIOS Reset Payload Request Register

When the BIOS software writes 0xA5 to this address, it will launch a payload request reset. If the related bit in the reset mark register is high, either a warm or cold reset will occur based on the reset function register bit.

Table 6-55 BIOS Reset Payload Request Register

Address Offset: 0x12			
Bit	Description	Default	Access
7:0	Writing magic word 0xA5 will cause a reset request	-	LPC: w

6.3.12.5 OS Reset Payload Request Register

The OS software writes 0x5A to this address and launches a payload reset request. If the related bit in Reset Mask Register is high, a warm o cold reset will occur based on the reset function register bit.

Table 6-56 OS Reset Payload Request Register

Address Offset: 0x13			
Bit	Description	Default	Access
7:0	Writing magic word 0x5A will cause a reset request	-	LPC: w

6.3.12.6 Payload Reset Source for IPMC Register

The IPMC Reset Source Register stores the source of the most recent reset. A "one" in the register bit indicates that the associated reset has occurred. If more than one reset occurs from different sources without clearing the corresponding register bits, one cannot determine the most recent reset source since more than one bit will be set. The same situation will occur is two reset sources are active at the same time.

Table 6-57 Payload Reset Source for IPMC Register

Address Offset: 0x14			
Bit	Description	Default	Access
0	Payload Power-on reset 1: Reset occurred	RST_N:1	IPMC: r/w1c
1	Reserved	0	IPMC: r/w1c
2	Front board push button reset payload request 1: Reset occurred	0	IPMC: r/w1c
3	IPMC reset payload request 1: Reset occurred	0	IPMC: r/w1c
4	RTM push button reset request 1: Reset occurred	0	IPMC: r/w1c
5	FPGA Watchdog reset payload request 1: Reset occurred	0	IPMC: r/w1c
6	BIOS reset payload request 1: Reset occurred	0	IPMC: r/w1c
7	OS reset payload request 1: Reset occurred	0	IPMC: r/w1c

6.3.12.7 Payload Reset Source for BIOS Register

The BIOS Reset Source Register stores the source of the most recent reset. A" one" in the register bit indicates that the associated reset has occurred. If more than one reset occurs from different sources without clearing the corresponding register bits, one can not determine the most recent reset source since more than one bit will be set. The same situation will happen if two reset sources go active at the same time.

The operating system should never write to this register.

Table 6-58 Payload Reset Source for BIOS Register

Address Offset: 0x15			
Bit	Description	Default	Access
0	Payload Power-on reset 1: Reset occurred	RST_N:1	LPC: r/w1c
1	Reserved	0	LPC: r/w1c
2	Front board push button reset payload request 1: Reset occurred	0	LPC: r/w1c
3	IPMC reset payload request 1: Reset occurred	0	LPC: r/w1c
4	RTM push button reset request 1: Reset occurred	0	LPC: r/w1c
5	FPGA Watchdog reset payload request 1: Reset occurred	0	LPC: r/w1c
6	BIOS reset payload request 1: Reset occurred	0	LPC: r/w1c
7	OS reset payload request 1: Reset occurred	0	LPC: r/w1c

6.3.12.8 Payload Reset Source for OS Register

The OS Reset Source Register stores the source of the most recent reset as it is done in the BIOS Reset Source Register. A "one" in the register bit indicates that the associated reset has occurred. If more than one reset occurs from different sources without clearing the corresponding register bits, one can not determine the most recent reset source since more than one bit will be set. The same situation will happen, if two reset sources go active at the same time.

Note: BIOS should never write to this register.

Table 6-59 Payload Reset Source for OS Register

Address Offset: 0x16			
Bit	Description	Default	Access
0	Payload Power-on reset 1: Reset occurred	RST_N:1	LPC: r/w1c
1	Reserved	0	LPC: r/w1c
2	Front board push button reset payload request 1: Reset occurred	0	LPC: r/w1c
3	IPMC reset payload request 1: Reset occurred	0	LPC: r/w1c
4	RTM push button reset payload request 1: Reset occurred	0	LPC: r/w1c
5	FPGA Watchdog reset payload request 1: Reset occurred	0	LPC: r/w1c
6	BIOS reset payload request 1: Reset occurred	0	LPC: r/w1c
7	OS reset payload request 1: Reset occurred	0	LPC: r/w1c

6.3.12.9 IPMC Watchdog Timeout Register

The IPMC SW sets the corresponding bit to signal an IPMC watchdog timeout event. When the IPMC Watchdog Timeout bit is set from low to high, the corresponding bits in Table 6-61 "IPMC Watchdog Timeout for BIOS Register" and Table 6-62 "IPMC Watchdog Timeout for OS Register" are set.

Table 6-60 IPMC Watchdog Timeout Register

Address Offset: 0x17			
Bit	Description	Default	Access
0	IPMC Watchdog Timeout 0: No IPMC Watchdog Timeout 1: IPMC Watchdog Timeout occurred	0	IPMC: r/w
1	IPMC Watchdog Pre-Timeout 0: No IPMC Watchdog Pre-Timeout 1: IPMC Watchdog Pre-Timeout occurred	0	IPMC: r/w
7:2	Reserved	000000	IPMC: r

6.3.12.10 IPMC Watchdog Timeout for BIOS Register

When the corresponding bits in *IPMC Watchdog Timeout Register* changes from 0 to 1, this register will have its bits set to 1. The BIOS software can clear certain bits by writing 1 to it.

This register is only used for communication between the IPMC and the BIOS software. FPGA will not use these bits by itself. OS should never write to this register.

Table 6-61 IPMC Watchdog Timeout for BIOS Register

Address Offset: 0x18			
Bit	Description	Default	Access
0	IPMC Watchdog Timeout 1: IPMC Watchdog Timeout occurred	0	LPC: r/w1c
1	IPMC Watchdog Pre-Timeout 1: IPMC Watchdog Pre-Timeout occurred	0	LPC: r/w1c
7:2	Reserved	000000	LPC: r

6.3.12.11 IPMC Watchdog Timeout for OS Register

When the corresponding bits in *IPMC Watchdog Timeout Register* changes from 0 to 1, this register will have its bits set to 1. The OS software can clear certain bits by writing 1 to it.

This register is only used for communication between the IPMC and the OS software. FPGA will not use these bits by itself. BIOS should never write to this register.

Table 6-62 IPMC Watchdog Timeout for OS Register

Address Offset: 0x19			
Bit	Description	Default	Access
0	IPMC Watchdog Timeout 1: IPMC Watchdog Timeout occurred	0	LPC: r/w1c
1	IPMC Watchdog Pre-Timeout 1: IPMC Watchdog Pre-Timeout occurred	0	LPC: r/w1c
7:2	Reserved	000000	LPC: r

6.3.12.12 FPGA-Payload-Watchdog Threshold Register

Payload software writes to this register to set the timeout threshold of a 16-bit internal watchdog reserved for future payload use. Unit is one msec, with a maximum time of 65535 ms. When "0" is written into it, the watchdog will be disabled and never bite.Address Offset:

Watchdog will be cleared each time when writing new threshold registers.

Watchdog will be cleared during power-up reset and cold reset.

Table 6-63 FPGA-Payload-Watchdog Threshold Low-byte Register

Address Offset: 0x1A			
Bit	Description	Default	Access
7:0	Low byte of timeout threshold for FPGA-Payload-Watchdog, unit is one msec	0xFF	LPC: r/w

0x1B

BitDescriptionDefaultAccess

7:0High byte of timeout threshold for FPGA-Payload-Watchdog, unit is one msec0xFFLPC: r/w

6.3.12.13 FPGA Payload Watchdog Clear Register

Any write done by the payload software to this register will be treated as feed and restarts the FPGA Payload Watchdog.

Table 6-64 FPGA-Payload-Watchdog Clear Register

Address Offset: 0x1C			
Bit	Description	Default	Access
7:0	Writing any data will clear the FPGA-Payload-Watchdog	-	LPC: w

6.3.12.14 FPGA-IPMC-Watchdog Threshold Register

The FPGA has an internal watchdog which monitors how the IPMC is normally running. If the IPMC fails to feed the FPGA according to the time set by this register, the latter will issue a cold reset to the former. Payload will not be affected by the reset of the IPMC).

The IPMC software writes this register to set the timeout threshold of the FPGA-IPMC Watchdog. Unit is one second, maximum time is 255s. When "0" is written to it, the watchdog will be disabled and will never bite. Writing and other data will enable and restart the FPGA-IPMC-Watchdog.

Table 6-65 FPGA-IPMC-Watchdog Threshold Register

Address Offset: 0x1F			
Bit	Description	Default	Access
7:0	Timeout threshold the 'FPGA-IPMC-Watchdog', unit is one second.	00	IPMC: r/w

6.3.13 Flash Control Register

Table 6-66 Flash Control Register

Address Offset: 0x40			
Bit	Description	Default	Access
0	Inverted of DEF_SPI_WP_N output 0: DEF_SPI_WP_N output high 1: DEF_SPI_WP_N output low	0	LPC: r IPMC:r/w
1	Inverted of REC_SPI_WP_N output 0: REC_SPI_WP_N output high 1: REC_SPI_WP_N output low	0	LPC: r IPMC:r/w
6:2	Reserved	00000	r
7	Payload Boot SPI Flash select. 0: Default Boot Flash linked to PCH, Recovery one to IPMC 1: Recovery Boot Flash linked to PCH, Default one to IPMC	0	LPC: r IPMC:r/w

6.3.14 RTM Status and Control Register

Table 6-67 RTM Status and Control Register

Address Offset: 0x4A			
Bit	Description	Default	Access
0	RTM_PS1_N	Ext.	r
1	RTM_ALL_PG	Ext.	r
2	RTM_MP_PG	Ext.	r
3	RTM_PP_PG	Ext.	r

Table 6-67 RTM Status and Control Register (continued)

Address Offset: 0x4A			
Bit	Description	Default	Access
4	FPGA_RTM_EN_N	1	LPC: r IPMC: r/w
5	FPGA_RTM_MP_EN	0	LPC: r IPMC: r/w
6	FPGA_RTM_PP_EN	0	LPC: r IPMC: r/w
7	Reserved	1	LPC: r IPMC: r/w

6.3.15 Blue LED Status and Control Register

Table 6-68 User LED Status and Control Register

Address Offset: 0x56			
Bit	Description	Default	Access
1:0	Software set Blue LED mode: 00: Solid on. 01: Long blinking. 10: Short blinking. 11: Off.	00	LPC: r IPMC: r/w
2	Blue LED master selection: 0: Software control Blue LED with bit1~0 setting in this register. 1: FPGA control Blue LED according to handle status (long blinking if handle is closed or solid on if it is open).	0	LPC: r IPMC: r/w
7:3	Reserved	00000	r

6.3.16 User LED Status and Control Register

Table 6-69 User LED Status and Control Register

Address Offset: 0x57			
Bit	Description	Default	Access
0	Control user LED #3 green color output Signal LED_USER3_GRN_N: 0: LED_USER3_GRN_N is driven high. 1: LED_USER3_GRN_N is driven low.	0	LPC: r/w IPMC: r
1	Control user LED #3 red color output Signal LED_USER3_RED_N: 0: LED_USER3_RED_N is driven high. 1: LED_USER3_RED_N is driven low.	0	LPC: r/w IPMC: r
2	Control user LED #1 red color output Signal LED_USER1_RED_N: 0: LED_USER1_RED_N is driven high. 1: LED_USER1_RED_N is driven low.	0	LPC: r/w IPMC: r
3	Control user LED #2 red color output Signal LED_USER2_RED_N: 0: LED_USER2_RED_N is driven high. 1: LED_USER2_RED_N is driven low.	0	LPC: r/w IPMC: r
4	Control BI LED enable output Signal LED_BI_EN_N: 0: LED_BI_EN_N is driven high. 1: LED_BI_EN_N is driven low.	0	r
7:5	Reserved	000	r

6.3.17 Miscellaneous Status and Control Register

The Miscellaneous register provides the status of hardware signals for IPMC to monitor, like the occupation status of both CPU sockets

Table 6-70 Miscellaneous Status and Control Register

Address Offset: 0x58			
Bit	Description	Default	Access
0	FRB_HDL_SW_N	Ext.	r
1	BMC_WDO_N	Ext.	r
3:2	CPU_SKTOCC_N[1:0]	Ext.	r
4	CPU_IVY_N	Ext.	r
5	PCH_HOT_N	Ext.	r
6	Reserved	0	r
7	IPMC to payload NMI request: 1: NMI active 0: NMI inactive Note: FPGA_PCH GPIO3 signal will also be controlled by warm-reset procedure	0	IPMC: r/w LPC: r

6.3.18 Debug Switch and LED Status Register

Table 6-71 Debug Switch and LED Status Register

Address Offset: 0x59			
Bit	Description	Default	Access
3:0	DBG_SW[3:0]	Ext.	r
7:4	FPGA_DBG_LED_N[3:0]	Ext.	r

6.3.19 Scratch Register

Table 6-72 LPC Scratch Registers

Address Offset: 0x76-7D			
Bit	Description	Default	Access
7:0	LPC Scratch bits.	0x00	LPC: r/w IPMC: r

6.3.20 POST Code Register

The FPGA provides an 8-bit wide register to store POST codes to the LPC I/O address 0x80. The two nibbles of the register are converted to seven segment codes and are displayed as two hex values by two seven-segment LED displays, which can be read by IPMC at SPI address 0x7F.

Table 6-73 POST Code Register

Address Offset: 0x7F			
Bit	Description	Default	Access
7:0	POST codes from host	0x00	IPMC: r

6.4 Standard Status Codes

Table 6-74 Component Status Codes

Status Code	Code Symbol
0x20	POSTCODE_CC_VARIABLE_SERVICES
0x21	POSTCODE_CC_KEYBOARD_CONTROLLER
0x22	POSTCODE_CC_BOOT_MODE
0x23	POSTCODE_CC_S3_SUPPORT

Table 6-74 Component Status Codes

Status Code	Code Symbol
0x24	POSTCODE_CC_TCG
0x25	POSTCODE_CC_HDD_PASSWORD
0x26	POSTCODE_CC_CPU_IO
0x27	POSTCODE_CC_BOOT_SCRIPT
0x28	POSTCODE_CC_STATUS_CODE
0x29	POSTCODE_CC_DATA_HUB
0x2A	POSTCODE_CC_HII_DATABASE
0x2B	POSTCODE_CC_RESET
0x2C	POSTCODE_CC_METRONOME
0x2D	POSTCODE_CC_INTERRUPT_CONTROLLER
0x2E	POSTCODE_CC_DIAGNOSTIC_SUMMARY
0x2F	POSTCODE_CC_SMBIOS
0x30	POSTCODE_CC_SMM_COMMUNICATION
0x31	POSTCODE_CC_SMM_RUNTIME
0x32	POSTCODE_CC_SMM_SERVICES
0x33	POSTCODE_CC_FIRMWARE_DEVICE
0x34	POSTCODE_CC_CAPSULE_SERVICES
0x35	POSTCODE_CC_MONOTONIC_COUNTER
0x36	POSTCODE_CC_SMBIOS_EVENT_LOG
0x37	POSTCODE_CC_RTC
0x38	POSTCODE_CC_BOOT_MANAGER
0x39	POSTCODE_CC_VGA
0x3A	POSTCODE_CC_HII_FORMS_BROWSER
0x3B	POSTCODE_CC_BOOT_MENU
0x3C	POSTCODE_CC_USER_MANAGER
0x3D	POSTCODE_CC_TIMER
0x3E	POSTCODE_CC_PCI_BUS

Table 6-74 Component Status Codes

Status Code	Code Symbol
0x3F	POSTCODE_CC_ISA_BUS
0x40	POSTCODE_CC_IDE_BUS
0x41	POSTCODE_CC_AHCI_BUS
0x42	POSTCODE_CC_SCSI_BUS
0x43	POSTCODE_CC_USB_BUS
0x44	POSTCODE_CC_FLOPPY
0x45	POSTCODE_CC_SERIAL_PORT
0x46	POSTCODE_CC_PS2_MOUSE
0x47	POSTCODE_CC_PS2_KEYBOARD
0x48	POSTCODE_CC_EHCI
0x49	POSTCODE_CC_XHCI
0x4A	POSTCODE_CC_UHCI
0x4B	POSTCODE_CC_OHCI
0x4C	POSTCODE_CC_USB_KEYBOARD
0x4D	POSTCODE_CC_USB_MOUSE
0x4E	POSTCODE_CC_USB_MASS_STORAGE
0x4F	POSTCODE_CC_CONSOLE_SPLITTER
0x50	POSTCODE_CC_GRAPHICS_CONSOLE
0x51	POSTCODE_CC_SERIAL_CONSOLE
0x52	POSTCODE_CC_TEXT_CONSOLE
0x53	POSTCODE_CC_DISK_IO
0x54	POSTCODE_CC_PARTITION
0x55	POSTCODE_CC_SETUP
0x56	POSTCODE_CC_LEGACY_BIOS
0x57	POSTCODE_CC_BLOCK_IO_THUNK
0x58	POSTCODE_CC_CRYPTO
0x59	POSTCODE_CC_XHCI_RESET

Table 6-74 Component Status Codes

Status Code	Code Symbol
0xA0	POSTCODE_CC_PLATFORM_STAGE0
0xA1	POSTCODE_CC_PLATFORM_STAGE1
0xA2	POSTCODE_CC_PLATFORM_STAGE2
0xA1	POSTCODE_CC_PLATFORM_SMM
0xA2	POSTCODE_CC_PLATFORM_FLASH
0xA3	POSTCODE_CC_PLATFORM_CSM
0xC0	POSTCODE_CC_MEMORY_CONTROLLER
0xC1	POSTCODE_CC_PCIE
0xC2	POSTCODE_CC_MANAGEMENT_ENGINE
0xC3	POSTCODE_CC_PCH
0xC4	POSTCODE_CC_SATA
0xD1	POSTCODE_CC_FLASH_CONTROLLER
0xD2	POSTCODE_CC_FLASH_DEVICE
0xD3	POSTCODE_CC_FINGERPRINT_SENSOR
0xD4	POSTCODE_CC_CLOCK_CONTROLLER
0xD5	POSTCODE_CC_EMBEDDED_CONTROLLER
0xD6	POSTCODE_CC_SERIAL_CONTROLLER

Table 6-75 Progress Status Codes

Status Code	Code Symbol
0x01	POSTCODE_PC_COMP_PEI_BEGIN
0x02	POSTCODE_PC_COMP_PEI_END
0x03	POSTCODE_PC_COMP_DXE_BEGIN
0x04	POSTCODE_PC_COMP_DXE_END
0x05	POSTCODE_PC_COMP_SUPPORTED
0x06	POSTCODE_PC_COMP_START
0x07	POSTCODE_PC_COMP_STOP

Table 6-75 Progress Status Codes

Status Code	Code Symbol
0x08	POSTCODE_PC_COMP_SMM_INIT
0x09	POSTCODE_EC_DEVICE_ERROR
0x0A	POSTCODE_EC_RESOURCE_ERROR
0x0B	POSTCODE_EC_DATA_CORRUPT

Table 6-76 Architectural Status Codes

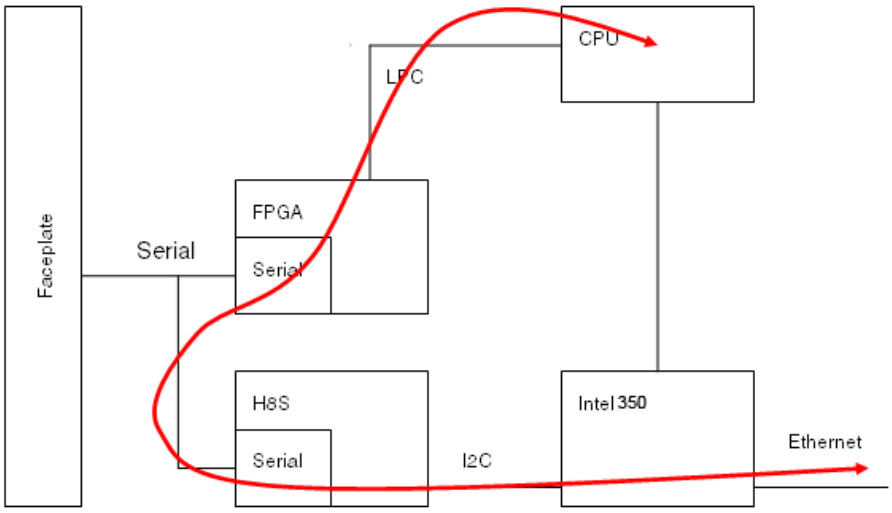
Status Code	Code Symbol
0xE0	POSTCODE_PC_SEC_ENTRY
0xE1	POSTCODE_PC_SEC_EXIT
0xE2	POSTCODE_PC_PEI_ENTRY
0xE3	POSTCODE_PC_PEI_EXIT
0xE4	POSTCODE_PC_IPL_DXE
0xE5	POSTCODE_PC_IPL_S3
0xE6	POSTCODE_PC_S3_OS
0xE7	POSTCODE_PC_IPL_RECOVERY
0xE8	POSTCODE_PC_IPL_EXIT
0xE9	POSTCODE_PC_DXE_ENTRY
0xEA	POSTCODE_PC_DXE_EXIT
0xEB	POSTCODE_EC_PEI_MEMORY
0xEC	POSTCODE_EC_PEI_IPL
0xED	POSTCODE_EC_IPL_DXE
0xEE	POSTCODE_EC_IPL_PPI
0xEF	POSTCODE_EC_DXE_ARCH

7.1 Overview

Serial Over LAN (SOL) is a mechanism that you can use to redirect the serial console from the blade via an IPMI session over the network. SOL uses the RMCP+ protocol.

The IPMC is used to establish and control the SOL session. SOL is only available on the base interface. The sideband interface of the Intel 350 (in pass-through mode) is used to transmit/receive its terminal characters via the base interface.

Figure 7-1 SOL Overview



You can configure the SOL parameters using the standard IPMI commands or via an open source tool called ipmitool.

7.2 Installing the ipmitool

You can download the open source tool ipmitool from http://ipmitool.sourceforge.net (at the time of publishing this manual the current version is 1.8.11). Documentation for this tool is also available on this site.

Procedure

To install the ipmitool, proceed as follows:

1. Download the ipmitool tar file from http://ipmitool.sourceforge.net to your blade.
2. Extract the source code.
   `prompt>tar -xjvf ipmitool-<version>.tar.bz2`
3. Go to the directory to which you have extracted the ipmitool.
   `prompt>cd <path>/ipmitool-<version>`
4. Build the ipmitool.
   `prompt>./configure && make && make install`

7.3 Configuring SOL Parameters

You can configure the following SOL parameters.

Table 7-1 SOL Parameters

Parameter	Description
Set LAN Configuration Parameter (IP address/MAC address)	Use this command to set the IP and MAC address.
Set Channel Access (Privilege level)	Use this command to set the privilege level.
Set User Name	Default value is soluser.
Set User Password	Default value is solpasswd.

You can use standard IPMI commands or the ipmitool to modify the parameters.

7.3.1 Using Standard IPMI Commands

This example shows how to set up the SOL configuration parameter with standard IPMI commands. Ipmicmd is used on the local IPMC and the IP is configured.

Sample Procedure

To set the IP address, proceed as follows:

1. Establish an IPMI connection to the blade.
2. Set LAN Configuration Parameter Set In Progress Lock.
   ipmicmd -k "f 0 c 1 1 0 1" smi 0
3. Set LAN Configuration Parameter Set IP (172.16.10.11 on channel 1).
   ipmicmd -k "f 0 c 1 1 3 ac 10 0a dd" smi 0
4. Set LAN Configuration Parameter Set In Progress Commit.
   ipmicmd -k "f 0 c 1 1 0 2" smi 0

7.3.2 Using ipmitool

The example below shows how to setup a LAN configuration parameter for a potential SOL session with ipmitool for base 1 (channel 1).

```
n0s70:~ #ipmitool lan set 1 ipaddr 172.16.0.221

Setting LAN IP Address to 172.16.0.221

n0s70:~ #
```

The following example shows how to query the LAN parameters that are currently in use for a potential SOL session for base 1(channel 1) and base 2(channel 2):

```
root@localhost:~# ipmitool lan print 1

Set in Progress         : Set Complete

Auth Type Support       :

Auth Type Enable        : Callback :

                        : User     :

                        : Operator :

                        : Admin    :
```

```
                          : OEM      :
IP Address Source         : Unspecified
IP Address                : 172.16.0.221
Subnet Mask               : 255.255.0.0
MAC Address               : 00:00:00:00:00:00
Default Gateway IP        : 172.16.0.1
Default Gateway MAC       : 00:00:00:00:00:00
RMCP+ Cipher Suites       : 1,2,3,3
Cipher Suite Priv Max     : Not Available
root@localhost:~# ipmitool lan print 2
Set in Progress           : Set Complete
Auth Type Support         :
Auth Type Enable          : Callback :
                          : User     :
                          : Operator :
                          : Admin    :
                          : OEM      :
IP Address Source         : Unspecified
IP Address                : 172.17.1.220
Subnet Mask               : 255.255.0.0
MAC Address               : 00:00:00:00:00:00
Default Gateway IP        : 172.17.0.1
Default Gateway MAC       : 00:00:00:00:00:00
```

```
RMCP+ Cipher Suites     : 1,2,3,3

Cipher Suite Priv Max   : Not Available

root@localhost:~#
```

MAC Address 00:00:00:00:00:00 means the address is shared between base and SOL interface. The address can be found out in the MAC address record of the FRU.

7.4 Establishing a SOL Session

To start a SOL session, the following requirements must be fulfilled:

- An Ethernet LAN connection to the onboard Gigabit Ethernet controller of the ATCA-7370 must exist.
- ATCA-7370 IPMC firmware must correspond to version 2.0.1 and above.

Procedure

To establish a SOL session, proceed as follows:

1. Make sure that the requirements detailed above are fulfilled.
2. Compile and install the ipmitool on your target which is destined for opening the SOL session on the ATCA-7370. For details refer to *Installing the ipmitool* on page 175.
3. Apply an IP address to the ATCA-7370 SOL interface. For details refer to *Configuring SOL Parameters* on page 176.
4. If necessary change user and password.
   Default user is "soluser" and password is "solpasswd".
5. Configure the network between the ATCA-7370 and your target, which is destined for opening the SOL session, so that the SOL IP address is accessible.

6. Start ATCA-7370 SOL session on your target with the ipmitool and the configured IP address for the ATCA-7370 SOL interface.
   `ipmitool -C 1 -I lanplus -H 172.16.0.221 -U soluser -P solpasswd -k gkey sol activate`
   For details on the command parameters, refer to the ipmitool documentation available on http://ipmitool.sourceforge.net.

To access BIOS setup screen, it is necessary to reset the payload. SOL session is only available if the payload is powered on and initialized by the BIOS.

Supported IPMI Commands

8.1 Standard IPMI Commands

The IPMC is fully compliant to the Intelligent Platform Management Interface v1.5. This section provides information about the supported IPMI commands.

8.1.1 Global IPMI Commands

The IPMC supports the following global IPMI commands.

Table 8-1 Supported Global IPMI Commands

Command	NetFn (Request/Response)	CMD
Get Device ID	0x06/0x07	0x01
Cold Reset	0x06/0x07	0x02
Warm Reset	0x06/0x07	0x03
Get Self Test Results	0x06/0x07	0x04
Get Device GUID	0x06/0x07	0x08

8.1.2 System Interface Commands

The IPMC supports the following IPMI commands to support the system messaging interfaces.

Table 8-2 Supported System Interface Commands

Command	NetFn (Request/Response)	CMD
Set BMC Global Enables	0x06/0x07	0x2E
Get BMC Global Enables	0x06/0x07	0x2F
Clear Message Flags	0x06/0x07	0x30
Get Message Flags	0x06/0x07	0x31
Get Message	0x06/0x07	0x33
Send Message	0x06/0x07	0x34
Set Channel Access	0x06/0x07	0x40

Table 8-2 Supported System Interface Commands (continued)

Command	NetFn (Request/Response)	CMD
Get Channel Access	0x06/0x07	0x41
Get Channel Info	0x06/0x07	0x42
Set User Access	0x06/0x07	0x43
Get User Access	0x06/0x07	0x44
Set User Name	0x06/0x07	0x45
Get User Name	0x06/0x07	0x46
Set User Password	0x06/0x07	0x47
Set User Payload Access	0x06/0x07	0x4C
Get User Payload Access	0x06/0x07	0x4D
Master Write-Read	0x06/0x07	0x52
Set Channel Security Keys	0x06/0x07	0x56

8.1.3 BMC Watchdog Commands

The watchdog commands are supported by blades providing a system interface and a watchdog type 2 sensor.

The options of pre-timeout and power-cycle are not supported.

Table 8-3 Supported Watchdog Commands

Command	NetFn (Request/Response)	CMD
Reset Watchdog Timer	0x06/0x07	0x22
Set Watchdog Timer	0x06/0x07	0x24
Get Watchdog Timer	0x06/0x07	0x25

8.1.4 SEL Device Commands

Table 8-4 Supported SEL Device Commands

Command	NetFn (Request/Response)	CMD
Get SEL Info	0x0A/0x0B	0x40
Reserve SEL	0x0A/0x0B	0x42
Get SEL Entry	0x0A/0x0B	0x43
Add SEL Entry	0x0A/0x0B	0x44
Clear SEL	0x0A/0x0B	0x47
Get SEL Time	0x0A/0x0B	0x48
Set SEL Time	0x0A/0x0B	0x49

8.1.5 FRU Inventory Commands

Table 8-5 Supported FRU Inventory Commands

Command	NetFn (Request/Response)	CMD
Get FRU Inventory Area Info	0x0A/0x0B	0x10
Read FRU Data	0x0A/0x0B	0x11
Write FRU Data	0x0A/0x0B	0x12

8.1.6 Sensor Device Commands

Table 8-6 Supported Sensor Device Commands

Command	NetFn (Request/Response)	CMD
Get Device SDR Info	0x04/0x05	0x20
Get Device SDR	0x04/0x05	0x21
Reserve Device SDR Repository	0x04/0x05	0x22
Get Sensor Reading Factors	0x04/0x05	0x23
Set Sensor Hysteresis	0x04/0x05	0x24
Get Sensor Hysteresis	0x04/0x05	0x25
Set Sensor Threshold	0x04/0x05	0x26
Get Sensor Threshold	0x04/0x05	0x27
Set Sensor Event Enable	0x04/0x05	0x28
Get Sensor Event Enable	0x04/0x05	0x29
Get Sensor Event Status	0x04/0x05	0x2B
Get Sensor Reading	0x04/0x05	0x2D
Get Sensor Type	0x04/0x05	0x2F

8.1.7 Chassis Device Commands

Table 8-7 Supported Chassis Device Commands

Command	NetFn (Request/Response)	CMD
Chassis Control	0x00/0x01	0x02
Set System Boot Options	0x00/0x01	0x08
Get System Boot Options	0x00/0x01	0x09

8.1.7.1 System Boot Options Commands

The Set system boot options commands allow you to control the boot process of a blade by setting boot parameters of the blade's boot firmware (BIOS). The boot firmware interprets the boot parameters and executes the boot process accordingly. Each boot parameter addresses a particular functionality and consists of one or more bytes. The parameters 0 to 7 are standard parameters defined by the IPMI specification. The And parameters, 96 to 127 are OEM-specific.

When using the Get/Set System Boot Options command with parameter selector of 96/97/98, the Set Selector and the Block Selector should be set to 0x00. When using the Get/Set System Boot Options command with parameter selector of 100, the Set Selector and the Block Selector have a specific meaning. Details are given in *System Boot Options Parameter #100* on page 188 for details.

The following table lists which boot properties can be configured and the corresponding boot parameter number.

Table 8-8 Configurable System Boot Option Parameters

Configurable Boot Property	Corresponding Boot Parameter Number
Selection between BIOS and FPGA boot	96
POST Type	97
Timeout for graceful shutdown	98
BIOS boot parameters	100

8.1.7.1.1 System Boot Options Parameter #96

This boot parameter is an Artesyn-specific OEM boot parameter as defined in the following table.

Table 8-9 System Boot Options Parameter #96

Data Byte	Description
1	1 Bits 7..2: Reserved Bit 1: FPGA configuration stream load 0: Load configuration stream from default boot flash 1: Load configuration stream from backup boot flash Note: The new FPGA configuration stream is loaded into the FPGA at the next power cycle of the payload
	Bit 0: Default/backup boot flash selection 0: Boot from default boot flash 1: Boot from backup boot flash Note: the newly selected boot flash is connected to the payload immediately, which means writing to the flash is possible. Its image is executed after the next power-up or cold reset of the payload.

The System Boot Options parameter #96 is non-volatile. It survives IPMC power cycle, reset and may survive the IPMC firmware upgrades.

NOTICE

Activating new upgraded IPMC firmware may lead to FPGA/BIOS boot bank change back to default boot bank if the NVRAM variables of the new upgraded IPMC firmware are different from the previous active version.

8.1.7.1.2 System Boot Options Parameter #97

This is an Artesyn-specific OEM parameter as defined in the following table.

Table 8-10 System Boot Options Parameter #97

Data Byte	Description
1	POST Type Data 1 - Set Selector. This is the processor ID for which the boot option is to be set.
2	Data 2 - POST Type Selector. This parameter is used to specify the POST type that the IPMC will execute. 0x00: Short POST 0x01: Long POST 0x02 to 0xFF: Not used

The System Boot Options parameter #97 is non-volatile. It survives the IPMC power cycle, reset and may survive the IPMC firmware upgrades.

8.1.7.1.3 System Boot Options Parameter #98

This is an Artesyn-specific OEM parameter.

It defines a timeout value for the graceful shutdown of the payload, which means how long the IPMC waits for the payload to shut down gracefully. If the payload software is not configured to be notified by the graceful shutdown requests, the IPMC will shut down the payload when the timer expires.

Table 8-11 System Boot Options Parameter #98

Bit	Description
15:8	Timeout for GRACEFUL_SHUTDOWN, MSB (given in 100 msec)
7:0	Timeout for GRACEFUL_SHUTDOWN, LSB (given in 100 msec)

The System Boot Options parameter #98 is non-volatile. It survives the IPMC power cycle, reset and may survive the IPMC firmware upgrades.

8.1.7.1.4 System Boot Options Parameter #100

The system boot options parameter #100 can be used to configure the blade's boot firmware and thus control the boot process. The boot options that can be configured using this parameter are typically a subset of the boot options which you can configure in the boot firmware directly, for example, using a setup menu.

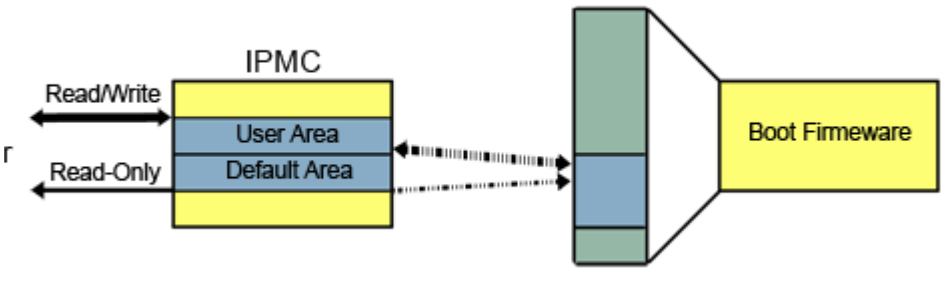
The IPMC contains a storage area for the payload boot options. When the blade boots, the boot firmware reads out these boot options from the IPMC, interprets them and executes the boot process accordingly. Note that the boot options stored in the IPMC have higher priority than that stored in the local area of the boot firmware itself.

The storage area for the boot options in the IPMC is divided into two parts: the default area and the user area. The user area is readable and settable. It contains the boot options that are used by the boot firmware during the boot process. The default area is readable only. It contains the default value of the boot options and is used to rollback the user area in case of mis-configuration. To load the default settings can be done typically by an on-board switch to clear the CMOS. The number of boot options stored in the IPMC may differ from project to project.

Changing a boot option in the firmware setup menu changes the boot option in the user area as well, if the same option is defined both in the user area and the set-up menu. Details are given below.

The following figure explains the basic information flow related to the system boot options parameter #100.

Figure 8-1 System Boot Options Parameter #100 - Information Flow Overview



The boot options are stored in the form of as a sequence of zero terminated strings. The following table describes in detail the format of the parameter data for the System Boot Options parameter #100.

Table 8-12 System Boot Options - Parameter #100 - Data Format

Byte	Description
0..1	Number of bytes of the boot options (LSB first) The number of bytes must be calculated and written into this field by the software which writes boot options into the storage area. The values of 0x0000 and 0xFFFF indicate that no valid data in the storage area.
2 .. n	Boot options The boot options are stored in the form of ASCII texts with the following format: <name>=<value>, where all name/value pairs are separated by one zero byte. The end of the boot parameter data is indicated by two zero bytes. Supported name/value pairs are blade-specific. Details are given below.
n + 1 .. n + 2	16 bit zero checksum of the boot options data section (LSB first).

Set Selector and Block Selector are used for the convenience of read/write of the boot options. Set Selector is used to select the storage area, default area or user area. The Block Selector is used to specify the offset into the storage area of the boot options in multiples of 16 bytes.

Table 8-13 System Boot Options Parameter #100 - SET Command Usage

Byte	Description
Request Data	
1	Parameter Selector [7] - 1b = the storage area is locked. 0b = the storage area is unlocked [6:0] - parameter selector (must be 100).
2	Set Selector 0h = user area All other values are reserved.

Table 8-13 System Boot Options Parameter #100 - SET Command Usage (continued)

Byte	Description
3	Block Selector Offset into the storage area of the boot options in multiples of 16 bytes.
4 .. n (n <= 19)	Boot Options Data to be written. Should not exceed 16 bytes to be written at a time.
Response Data	
1	Completion Code. Generic plus the following command-specific completion codes: 80h = parameter not supported 81h = storage area is locked by another software entity 82h = illegal write-access

Table 8-14 System Boot Options Parameter #100 - GET Command Usage

Byte	Description
Request Data	
1	Parameter Selector [7] - reserved [6:0] - parameter selector (must be 100).
2	Set Selector 0h = user area 1h = default area All other values are reserved.
3	Block Selector Offset into the storage area of the boot options in multiples of 16 bytes.
Response Data	
1	Completion Code. Generic plus the following command-specific completion codes: 80h = parameter not supported

Table 8-14 System Boot Options Parameter #100 - GET Command Usage (continued)

Byte	Description
2	[7:4] - reserved [3:0] - parameter version. 1h is returned.
3	Parameter Valid [7] - 1b = the storage area is locked. 0b = the storage area is unlocked [6:0] - parameter selector (must be 100).
4 .. 19	Boot Option Data

To detect the size of the whole storage area, a series of read commands can be issued with the block selector in 1 increment. Once the error code C9 is returned, the limit has been reached and the total available space of the storage area can be determined by the block selector of the last issued command.

This is supported by HPI, for details refer to the *System Management Interface Based on HPI-B User's Guide* related to your system environment.

The following table lists the boot parameters that can be configured for the ATCA-7370 blade using the system boot option parameter #100.

Artesyn Embedded Technologies provides the tool "named ipmibpar", which is included in the BBS, to interpret the boot options stored in the IPMC.

The boot parameters and their values mentioned here are all case-sensitive.

All boot options listed in the following table are set by the BIOS setup menu and can be configured using the System Boot options command #100. The IPMC and BIOS software automatically synchronize the settings made in the BIOS setup menu and the settings specified using the System Boot Options command #100. Changing a parameter in either of these, automatically changes the respective value in the other.

Table 8-15 System Boot Options Parameter #100 - Supported Parameters

Parameter	Options	Default values
reset_type	warm:cold	warm
warmresetcnt	numeric(1~65535)	100
com_term_type	ansi:vt100:vt100+:utf8	vt100
baudrate	9600:19200:38400:57600:115200	115200
frontnet_boot	on:off	off
basenet_boot	on:off	on
artm_sas_boot	on:off	on
usb_boot	on:off	on
bios_wdt	on:off	on
bios_wdt_timeout	numeric(180~6000)	180
os_boot_wdt	on:off	on
os_boot_wdt_timeout	numeric(180~6000)	2400
en_cmp	all:1:2:3:4:5:6:7	all
en_ht	on:off	on
flexratio	on:off	off
ratio_value	numeric(12~30)	18
en_xd	on:off	off
virtualization	on:off	on
speedstep	on:off	on
turbo_mode	on:off	off
c_states	on:off	on
vtd_support	on:off	on
clk_spreadspec	on:off	on
artm_pwr_policy	on:off	off
ddr3_refresh	auto:7.8:3.9	auto
ddr3_vdd_limit	auto:1.5	auto
ecc_support	on:off	on

Table 8-15 System Boot Options Parameter #100 - Supported Parameters (continued)

Parameter	Options	Default values
ecc_log_option	off:ce:ue:both	both
celog_threshold	numeric(1~32767)	1
ceflood_threshold	numeric(1~65535)	20
usb1	on:off	on
usb2	on:off	on
rtm_usb	on:off	on
smbios_event_log	on:off	on
boot_order	boot_option_1	usbcdrom
	boot_option_2	usbfdd
	boot_option_3	usb1, usb2, usbartm
	boot_option_4	basenet0, basenet1
	boot_option_5	sashdd
	boot_option_6	frontnet0 frontnet1

Table 8-16 boot_order Devices

Device	Description
sashdd	SAS HDD mounted on the RTM
frontnet	Front Panel Network
basenet0	Base0 Network
basenet1	Base1 Network
usb1	USB frontpanel 1
usb2	USB frontpanel 2
usbartm	USB artm
usbcdrom	USB cdrom
usbfdd	USB floppy disk
efishell	Built in UEFI shell

8.1.8 Event Commands

Table 8-17 Supported Event Commands

Command	NetFn (Request/Response)	CMD
Set Event Receiver	0x04/0x05	0x00
Get Event Receiver	0x04/0x05	0x01
Platform Event	0x04/0x05	0x02

8.1.9 LAN Device Commands

Table 8-18 Supported LAN Device Commands

Command	NetFn (Request/Response)	CMD
Set LAN Configuration Parameters	0x0C/0x0D	0x01
Get LAN Configuration Parameters	0x0C/0x0D	0x02
Set SOL Configuration Parameters	0x0C/0x0D	0x21
Get SOL Configuration Parameters	0x0C/0x0D	0x22

8.2 PICMG 3.0 Commands

The Artesyn Embedded Technologies IPMC is a fully compliant AdvancedTCA Intelligent Platform Management Controller. It supports all required and mandatory AdvancedTCA commands as defined in the PICMG 3.0 R3.0 specification and AMC.0 R2.0 specification.

Table 8-19 Supported PICMG 3.0 Commands

Command	NetFn (Request/Response)	CMD
Get PICMG Properties	0x2C/0x2D	0x00
Get Address Info	0x2C/0x2D	0x01
FRU Control	0x2C/0x2D	0x04
Get FRU LED Properties	0x2C/0x2D	0x05
Get FRU LED Color Capabilities	0x2C/0x2D	0x06
Set FRU LED State	0x2C/0x2D	0x07
Get FRU LED State	0x2C/0x2D	0x08
Set IPMB State	0x2C/0x2D	0x09
Set FRU Activation Policy	0x2C/0x2D	0x0A
Get FRU Activation Policy	0x2C/0x2D	0x0B
Set FRU Activation	0x2C/0x2D	0x0C
Get Device Locator Record ID	0x2C/0x2D	0x0D
Set Port State	0x2C/0x2D	0x0E
Get Port State	0x2C/0x2D	0x0F
Compute Power Properties	0x2C/0x2D	0x10
Set Power Level	0x2C/0x2D	0x11
Get Power Level	0x2C/0x2D	0x12
Get IPMB Link Info	0x2C/0x2D	0x18
Set AMC Port State	0x2C/0x2D	0x19
Get AMC Port State	0x2C/0x2D	0x1A
Get FRU Control Capabilities	0x2C/0x2D	0x1E
Get target upgrade capabilities	0x2C/0x2D	0x2E

Table 8-19 Supported PICMG 3.0 Commands (continued)

Command	NetFn (Request/Response)	CMD
Get component properties	0x2C/0x2D	0x2F
Abort firmware upgrade	0x2C/0x2D	0x30
Initiate upgrade action	0x2C/0x2D	0x31
Upload firmware block	0x2C/0x2D	0x32
Finish firmware upload	0x2C/0x2D	0x33
Get upgrade status	0x2C/0x2D	0x34
Activate firmware	0x2C/0x2D	0x35
Query self-test results	0x2C/0x2D	0x36
Query rollback status	0x2C/0x2D	0x37
Initiate manual rollback	0x2C/0x2D	0x38

The firmware upgrade commands supported by the blade are implemented according to the PICMG HPM.1 Revision 1.0 specification.

The boot block can be updated with PICMG HPM.1 specific commands.

8.3 Artesyn Embedded Technologies Specific Commands

The Artesyn Embedded Technologies IPMC supports several commands which are not defined in the IPMI or PICMG 3.0 specification but are introduced by Artesyn Embedded Technologies: serial output commands.

- Before sending any of these commands, the shelf management software must check whether the receiving IPMI controller supports Artesyn Embedded Technologies specific IPMI commands by using the IPMI command 'Get Device ID'. Sending Artesyn Embedded Technologies specific commands to IPMI controllers which do not support these IPMI commands will lead to no or undefined results.
- Proper handling of these commands is required to write a portable application.

8.3.1 Set/Get Feature Configuration Commands

This command can be used to enable/disable features within the IPMC during runtime.

Table 8-20 Set/Get Feature Configuration Commands

Command Name	NetFn (Request/Response)	CMD	Description
Set Feature Configuration	0x2E/0x2F	0x1E	
Get Feature Configuration	0x2E/0x2F	0x1F	

8.3.1.1 Set Feature Configuration Command

This command can be used to set the IPMI feature.

Table 8-21 Set Feature Configuration Command

	Byte	Data Field
Request Data	1:3	Artesyn IANA Number (0065CDh). LSB first.
	4	Feature Selector. For details, please see Table "Feature Selector Assignments" on page 200
	5	Feature Configuration 00h = disabled (Feature Selector = E2h) 01h = enabled (Feature Selector = E2h)-Default 02h - FFh = reserved
	6	Persistency / Duration 00h = volatile. Actual duration depends on implementation. 01h - FFh = reserved
Response Data	1	Completion Code. Generic plus the following command-specific completion codes: 80h = feature selector not supported. 81h = feature configuration not supported 82h = configuration persistency / duration not supported
	2:4	Artesyn IANA Number (0065CDh). LSB first.

8.3.1.2 Get Feature Configuration Command

This command can be used to retrieve the IPMI feature set being configured.

Table 8-22 Get Feature Configuration Command

	Byte	Data Field
Request Data	1:3	Artesyn IANA Number (0065CDh). LSB first.
	4	Feature Selector, for details see Table 8-23 on page 200.

Table 8-22 Get Feature Configuration Command (continued)

	Byte	Data Field
Response Data	1	Completion Code. Generic plus the following command-specific completion codes: 80h = feature selector not supported.
	2:4	Artesyn IANA Number (0065CDh). LSB first.
	5	Feature Configuration
	6	Persistency / Duration

Table 8-23 Feature Selector Assignments

Feature Selector	Description
E2h	Boot Firmware Automatic Switchover Function Enable/Disable

8.3.2 Serial Output Commands

Table 8-24 Serial Output Commands

Command Name	NetFn (Request/Response)	CMD	Description
Set Serial Output	0x2E/0x2F	0x15	See *Set Serial Output Command* on page 201
Get Serial Output	0x2E/0x2F	0x16	See *Get Serial Output Command* on page 201

8.3.2.1 Set Serial Output Command

The Set Serial Output command selects the serial port output source for a serial port connector. The following table lists the request and response data applicable to the Set Serial Output command.

Table 8-25 Set Serial Output Command

	Byte	Data Field
Request Data	1:3	Artesyn IANA Number (0065CDh). LSB first.
	4	Serial connector type: 0 = Front panel connector 1 = Backplane connector All other values are reserved.
	5	Serial connector instance number, a value of 00h shall be used all other values are reserved
	6	Serial output selector. 0 = payload interface 2 = IPMC debug console All other values are reserved
Response Data	1	Completion code.
	2:4	Artesyn IANA Number (0065CDh). LSB first.

8.3.2.2 Get Serial Output Command

The Get Serial Output Command provides a way to determine which serial output source goes to a particular serial port connector.

Currently, only BIOS output is supported.

The following table lists the request and response data applicable to the Get Serial Output command.

Table 8-26 Get Serial Output Command

	Byte	Data Field
Request Data	1:3	Artesyn IANA Number (0065CDh). LSB first.
	4	Serial connector type: 0 = Front panel connector 1 = Backplane connector All other values are reserved.
	5	Serial connector instance number. A value of 00h shall be used all other values are reserved
Response Data	1	Completion code.
	2:4	Artesyn IANA Number (0065CDh). LSB first.
	5	Serial output selector. 0 = payload interface All other values are reserved

8.3.3 OEM Set/Get ACPI Power Commands

This command can be used to change payload's power state.

Table 8-27 OME Set/Get ACPI Power Commands

Command name	NetFn (Request/Response)	CMD	Description
OEM Set ACPI Power State	0x2E/0x2F	0x17	
OEM Get ACPI Power State	0x2E/0x2F	0x18	

8.3.3.1 OEM Set ACPI Power State (0x17)

Table 8-28 OEM Set ACPI Power State Command

	Byte	Data Field
Request Data	1	LSB of Artesyn IANA Enterprise Number. A value of CDh shall be used.
	2	2nd byte of Artesyn IANA Enterprise Number. A value of 65h shall be used.
	3	MSB of Artesyn IANA Enterprise Number. A value of 00h shall be used.
	4	ACPI System Power State to set Power states are mutually exclusive. Only one state can be set at a time. [7] - 1b set system power state, always with 1 [6:1] - Reserved [0] - System Power State enumeration --00h set S0 working --01h set S3 typically equates to "suspend-to-RAM"
Response Data	1	Completion Code. Generic completion codes:
	2	LSB of Artesyn IANA Enterprise Number. A value of CDh shall be used.
	3	2nd byte of Artesyn IANA Enterprise Number. A value of 65h shall be used.
	4	MSB of Artesyn IANA Enterprise Number. A value of 00h shall be used.

8.3.3.2 OEM Get ACPI Power State (0x18)

This command can be used to retrieve current ACPI power state.

Table 8-29 OEM Get ACPI Power State Command

	Byte	Data Field
Request Data	1	LSB of Artesyn IANA Enterprise Number. A value of CDh shall be used.
	2	2nd byte of Artesyn IANA Enterprise Number. A value of 65h shall be used.
	3	MSB of Artesyn IANA Enterprise Number. A value of 00h shall be used.
Response Data	1	Completion Code.
	2	LSB of Artesyn IANA Enterprise Number. A value of CDh shall be used.
	3	2nd byte of Artesyn IANA Enterprise Number. A value of 65h shall be used.
	4	MSB of Artesyn IANA Enterprise Number. A value of 00h shall be used.
	5	ACPI System Power State [7:2] - reserved [1:0] - System Power State enumeration --00h set S0 working --01h set S3 typically equates to "suspend-to-RAM" --02h S5 soft off --03h unknown

8.3.4 OEM Set/Get Performance Commands

Table 8-30 OEM Set/Get Performance Commands

Command name	NetFn (Request/Response)	CMD	Description
OEM Set Performance Mode	0x2E/0x2F	0x21	

Table 8-30 OEM Set/Get Performance Commands

Command name	NetFn (Request/Response)	CMD	Description
OEM Get Performance Mode	0x2E/0x2F	0x22	

8.3.4.1 OEM Set Performance Mode (0x21)

This command can be used to change the performance mode through the P-State of CPU, including normal performance mode and reduced performance mode.

Table 8-31 OEM Set Performance Mode Command

	Byte	Data Field
Request Data	1	LSB of NSN IANA Enterprise Number. A value of 2Ah shall be used.
	2	2nd byte of NSN IANA Enterprise Number. A value of 6Fh shall be used.
	3	MSB of NSN IANA Enterprise Number. A value of 00h shall be used.
	4	00h-0Fh = FRU ID, 0h for ACPI5-A
	5	Power performance mode level [7:1] - Reserved [0] - Power State Mode Level --0h normal performance mode --1h reduced performance mode
Response Data	1	Completion Code. Generic completion codes: 81h=failed to change performance mode 82h=already in the desired performance mode
	2	LSB of NSN IANA Enterprise Number. A value of 2Ah shall be used.
	3	2nd byte of NSN IANA Enterprise Number. A value of 6Fh shall be used.
	4	MSB of NSN IANA Enterprise Number. A value of 00h shall be used.

8.3.4.2 OEM Get Performance Mode (0x22)

This command can be used to retrieve current performance mode.

Table 8-32 OEM Get Performance Mode Command

	Byte	Data Field
Request Data	1	LSB of NSN IANA Enterprise Number. A value of 2Ah shall be used.
	2	2nd byte of NSN IANA Enterprise Number. A value of 6Fh shall be used.
	3	MSB of NSN IANA Enterprise Number. A value of 00h shall be used.
	4	00h-0Fh = FRU ID, 0h for ACPI5-A
Response Data	1	Completion Code.
	2	LSB of NSN IANA Enterprise Number. A value of 2Ah shall be used.
	3	2nd byte of NSN IANA Enterprise Number. A value of 6Fh shall be used.
	4	MSB of NSN IANA Enterprise Number. A value of 00h shall be used.
	5	Power performance mode: [7:1] - Reserved [0] - Power State Mode Level --0h normal performance mode --1h reduced performance mode
	6:7	Power draw value of reduced performance mode, the unit is watt, LS byte first.
	8:9	Power draw value of normal performance mode, the unit is watt, LS byte first.

8.4 Pigeon Point Specific Commands

The IPMC supports additional IPMI commands that are specific to Pigeon Point. This section provides detailed descriptions of those extensions:

Table 8-33 Pigeon Point Extension Commands

Command	NetFn (Request/Response)	CMD
Get Status Table 8-35 on page 208	0x2E/0x2F	0x00
Get Serial Interface Properties Table 8-36 on page 211	0x2E/0x2F	0x01
Set Serial Interface Properties Table 8-37 on page 212	0x2E/0x2F	0x02
Get Debug Level Table 8-38 on page 213	0x2E/0x2F	0x03
Set Debug Level Table 8-39 on page 214	0x2E/0x2F	0x04
Get Hardware Address Table 8-40 on page 215	0x2E/0x2F	0x05
Set Hardware Address Table 8-41 on page 215	0x2E/0x2F	0x06
Get Handle Switch Table 8-42 on page 216	0x2E/0x2F	0x07
Set Handle Switch Table 8-43 on page 217	0x2E/0x2F	0x08
Get Payload Communication Time-Out Table 8-44 on page 217	0x2E/0x2F	0x09
Set Payload Communication Time-Out Table 8-45 on page 218	0x2E/0x2F	0x0A
Enable Payload Control Table 8-46 on page 219	0x2E/0x2F	0x0B
Disable Payload Control Table 8-47 on page 219	0x2E/0x2F	0x0C
Reset IPMC Table 8-48 on page 220	0x2E/0x2F	0x0D
Hang IPMC Table 8-49 on page 220	0x2E/0x2F	0x0E
Graceful Reset Table 8-50 on page 221	0x2E/0x2F	0x11
Get Payload Shutdown Time-Out Table 8-51 on page 222	0x2E/0x2F	0x15
Set Payload Shutdown Time-Out Table 8-52 on page 223	0x2E/0x2F	0x16
Get Module State Table 8-53 on page 223	0x2E/0x2F	0x27
Enable Module Site Table 8-54 on page 225	0x2E/0x2F	0x28
Disable Module Site Table 8-55 on page 225	0x2E/0x2F	0x29

Table 8-33 Pigeon Point Extension Commands (continued)

Command	NetFn (Request/Response)	CMD
Reset Carrier SDR repository Table 8-56 on page 226	0x2E/0x2F	0x33

Some of the following commands refer to IPMC modes which are defined as follows:

Table 8-34 IPMC Modes

Mode	Description
Standalone	In standalone mode, the carrier IPMC disconnects from IPMB-0 but keeps on listening to the serial debug and payload interfaces and serving requests coming from them, as well as managing the modules, AMC point-to-point (P2P) and clock E-keying. Standalone mode is intended for debugging purposes and/or operation in a non-ATCA environment. In standalone mode, the carrier IPMC automatically activates and deactivates the on-carrier payload and modules whenever it does not violate any carrier limitations.
Manual standalone	Manual standalone mode is equivalent to standalone mode with only one exception: carrier IPMC control over the on-carrier payload is automatically disabled in manual standalone mode.

8.4.1 Get Status Command

The Get Status command can be used by the payload software to retrieve the status of the IPMC.

Table 8-35 Get Status Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00

Table 8-35 Get Status Command Description (continued)

Type	Byte	Data Field
	5	Bit [7] Graceful Reboot Request If set to "1", indicates that the payload is requested to initiate the graceful reboot sequence. Bit [6] Diagnostic Interrupt Request If set to "1", indicates that a payload diagnostic interrupt request has arrived. Bit [5] Shutdown Alert If set to "1", indicates that the payload is going to be shutdown. Bit [4] Reset Alert If set to "1", indicates that the payload is going to be reset. Bit [3] Sensor Alert If set to "1", indicates that at least one of the IPMC sensors detects a threshold crossing. Bits [2:1] Mode The current IPMC modes are defined as: 0: Normal 1: Standalone, for a description refer to Table 8-34 2: Manual Standalone, for a description refer to Table 8-34 Bit [0] Control If set to 0, the IPMC control over the payload is disabled.
	6	Bits [4:7] Metallic Bus 2 Events These bits indicate pending Metallic Bus 2 requests arrived from the shelf manager: 0: Metallic Bus 2 Query 1: Metallic Bus 2 Release 2: Metallic Bus 2 Force 3: Metallic Bus 2 Free Bits [0:3] Metallic Bus 1 Events These bits indicate pending Metallic Bus 1 requests arrived from the shelf manager: 0: Metallic Bus 1 Query 1: Metallic Bus 1 Release 2: Metallic Bus 1 Force 3: Metallic Bus 1 Free

Table 8-35 Get Status Command Description (continued)

Type	Byte	Data Field
	7	Bits [4:7] Clock Bus 2 Events These bits indicate pending Clock Bus 2 requests arrived from the shelf manager: 0: Clock Bus 2 Query 1: Clock Bus 2 Release 2: Clock Bus 2 Force 3: Clock Bus 2 Free Bits [0:3] Clock Bus 1 Events These bits indicate pending Clock Bus 1 requests arrived from the shelf manager: 0: Clock Bus 1 Query 1: Clock Bus 1 Release 2: Clock Bus 1 Force 3: Clock Bus 1 Free
	8	Bits [4:7] Reserved Bits [0:3] Clock Bus 3 Events These bits indicate pending Clock Bus 3 requests arrived from the shelf manager: 0: Clock Bus 3 Query 1: Clock Bus 3 Release 2: Clock Bus 3 Force 3: Clock Bus 3 Free

8.4.2 Get Serial Interface Properties Command

The Get Serial Interface Properties command is used to get the properties of a particular serial interface.

Table 8-36 Get Serial Interface Properties Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
	4	Interface ID 0: Serial Debug Interface
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00
	5	Bit [7] Echo On If this bit is set, the IPMC enables echo for the given serial interface. Bits [6:4] Reserved Bits [3:0] Baud Rate ID The baud rate ID defines the interface baud rate as follows: 0: 9600 bps 1: 19200 bps 2: 38400 bps 3: 57600 bps (unsupported) 4: 115200 bps (unsupported)

8.4.3 Set Serial Interface Properties Command

The Set Serial Interface Properties command is used to set the properties of a particular serial interface.

Table 8-37 Set Serial Interface Properties Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
	4	Interface ID 0: Serial Debug Interface
	5	Bit [7] Echo On If this bit is set, the IPMC enables echo for the given serial interface. Bits [6:4] Reserved Bits [3:0] Baud Rate ID The baud rate ID defines the interface baud rate as follows: 0: 9600 bps 1: 19200 bps 2: 38400 bps 3: 57600 bps (unsupported) 4: 115200 bps (unsupported)
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00

8.4.4 Get Debug Level Command

The Get Debug Level command gets the current debug level of the IPMC firmware.

Table 8-38 Get Debug Level Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00
	5	Bit [7] IPMB-L Dump Enable If set to 1, the IPMC provides a trace of IPMB-L messages that are arriving to/going from the IPMC via IPMB-L. Bit [6] n/a Bit [5] KCS Dump Enable If set to "1", the IPMC provides a trace of KCS messages that are arriving to/going from the IPMC via KCS. Bit [4] IPMB Dump Enable If set to "1", the IPMC provides a trace of IPMB messages that are arriving to/going from the IPMC via IPMB-O. Bit [3] n/a Bit [2] Alert Logging Enable If set to "1", the IPMC outputs important alert messages onto the serial debug interface. Bit [1] Low-level Error Logging Enable If set to "1", the IPMC outputs low-level error/diagnostic messages onto the serial debug interface. Bit [0] Error Logging Enable If set to "1", the IPMC outputs error/diagnostic messages onto the serial debug interface.

8.4.5 Set Debug Level Command

The Set Debug Level command sets the current debug level of the IPMC firmware.

Table 8-39 Set Debug Level Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
	4	Bit [7] IPMB-L Dump Enable If set to "1", the IPMC provides a trace of IPMB-L messages that are arriving to/going from the IPMC via IPMB-L. Bit [6] n/a Bit [5] KCS Dump Enable If set to "1", the IPMC provides a trace of KCS messages that are arriving to/going from the IPMC via KCS. Bit [4] IPMB Dump Enable If set to "1", the IPMC provides a trace of IPMB messages that are arriving to/going from the IPMC via IPMB-O. Bit [3] n/a Bit [2] Alert Logging Enable If set to "1", the IPMC outputs important alert messages onto the serial debug interface. Bit [1] Low-level Error Logging Enable If set to "1", the IPMC outputs low-level error/diagnostic messages onto the serial debug interface. Bit [0] Error Logging Enable If set to "1", the IPMC outputs error/diagnostic messages onto the serial debug interface.
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00

8.4.6 Get Hardware Address Command

The Get Hardware Address command reads the hardware address of the IPMC.

Table 8-40 Get Hardware Address Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00
	5	Hardware Address

8.4.7 Set Hardware Address Command

The Set Hardware Address command allows the user to override the hardware address read from the hardware when the IPMC operates in (manual) standalone mode (for a description refer to Table 8-34).

Table 8-41 Set Hardware Address Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
	4	Hardware Address If set to 00, the ability to override the hardware address is disabled. NOTE: A hardware address change only takes effect after an IPMC reset.
Response Data	1	Completion Code

Table 8-41 Set Hardware Address Command Description (continued)

Type	Byte	Data Field
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00

8.4.8 Get Handle Switch Command

The Get Handle Switch command reads the state of the hot-swap handle of the IPMC. Overriding of the handle switch state is allowed only if the IPMC operates in (manual) standalone mode (for a description refer to Table 8-34).

Table 8-42 Get Handle Switch Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00
	5	Handle Switch Status 0x00: The handle switch is open. 0x01: The handle switch is closed. 0x02: The handle switch state is read from hardware.

8.4.9 Set Handle Switch Command

The Set Handle Switch command sets the state of the hot-swap handle switch in (manual) standalone mode (for a description refer to Table 8-34).

Table 8-43 Set Handle Switch Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
	4	Handle Switch Status 0x00: The handle switch is open. 0x01: The handle switch is closed. 0x02: The handle switch state is read from hardware.
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00

8.4.10 Get Payload Communication Time-Out Command

The Get Payload Communication Time-Out command reads the payload communication time-out value.

Table 8-44 Get Payload Communication Time-Out Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00

Table 8-44 Get Payload Communication Time-Out Command Description (continued)

Type	Byte	Data Field
	5	Payload Time-out Payload communication time-out measured in hundreds of milliseconds. Thus, the payload communication time-out may vary from 0.1 to 25.5 seconds.

8.4.11 Set Payload Communication Time-Out Command

The Set Payload Communication Time-Out command sets the payload communication time-out value.

Table 8-45 Set Payload Communication Time-Out Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
	4	Payload Time-out Payload communication time-out measured in hundreds of milliseconds. Thus, the payload communication time-out may vary from 0.1 to 25.5 seconds.
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00

8.4.12 Enable Payload Control Command

The Enable Payload Control command enables payload control from the serial debug interface.

Table 8-46 Enable Payload Control Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00

8.4.13 Disable Payload Control Command

The Disable Payload Control command disables payload control from the serial debug interface.

Table 8-47 Disable Payload Control Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00

8.4.14 Reset IPMC Command

The Reset IPMC command allows the payload to reset the IPMC over the KCS host interface.

Table 8-48 Reset IPMC Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
	4	Reset Type Code 0x00: Cold IPMC reset to the current mode 0x01: Cold IPMC reset to the Normal mode 0x02: Cold IPMC reset to the Standalone mode, for a description refer to Table 8-34 0x03: Cold IPMC reset to the Manual Standalone mode, for a description refer to Table 8-34 0x04: Reset the IPMC and enter Upgrade mode
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00

8.4.15 Hang IPMC Command

The IPMC provides a way to test the watchdog timer support by implementing the Hang IPMC command, which simulates firmware hanging by entering an endless loop.

Table 8-49 Hang IPMC Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
Response Data	1	Completion Code

Table 8-49 Hang IPMC Command Description (continued)

Type	Byte	Data Field
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00

8.4.16 Graceful Reset Command

The IPMC supports the Graceful Reboot option of the FRU Control command. On receiving such a command, the IPMC sets the Graceful Reboot Request bit of the IPMC status, sends a status update notification to the payload, and waits for the Graceful Reset command from the payload. If the IPMC receives such a command before the payload communication time-out time, it sends the 0x00 completion code (Success) to the shelf manager. Otherwise, the 0xCC completion code is sent.

The IPMC does not reset the payload upon receiving the Graceful Reset command or time-out. If the IPMC participation is necessary, the payload must request the IPMC to perform a payload reset. The Graceful Reset command is also used to notify the IPMC about the completion of the payload shutdown sequence.

Table 8-50 Graceful Reset Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00

8.4.17 Get Payload Shutdown Time-Out Command

When the shelf manager commands the IPMC to shut down the payload (i.e. sends the Activate/Deactivate FRU command), the IPMC notifies the payload by forwarding the command Activate/Deactivate FRU to the KCS interface. Provided the OpenIPMI driver has registered this command for notification, the payload gets notified. Upon receiving this notification, the payload software is expected to initiate the payload shutdown sequence. After performing this sequence, the payload should send the Graceful Reset command to the IPMC over the payload Interface to notify the IPMC that the payload shutdown is complete.

To avoid deadlocks that may occur if the payload software does not respond, the IPMC provides a special time-out for the payload shutdown sequence. If the payload does not send the Graceful Reset command within a definite period of time, the IPMC assumes that the payload shutdown sequence is finished, and resets the payload.

Table 8-51 Get Payload Shutdown Time-Out Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00
	5:6	Time-Out measured in hundreds of milliseconds, LSB first

8.4.18 Set Payload Shutdown Time-Out Command

The Set Payload Shutdown Time-Out command is defined as follows.

Table 8-52 Set Payload Shutdown Time-Out Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
	4:5	Time-Out measured in hundreds of milliseconds, LSB first
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00

8.4.19 Get Module State Command

The Get Module State command is used to query the state of a module (RTM with site ID1) using any of the external interfaces.

Table 8-53 Get Module State Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
	4	Module Site ID
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00

Table 8-53 Get Module State Command Description (continued)

Type	Byte	Data Field
	5	Module Status Bit [0] 0: Module site is enabled. 1: Module site is disabled. Bit [1] 0: Module is not present. 1: Module is present. Bit [2] 0: Management power is disabled. 1: Management power is enabled. Bit [3] 0: Management power is bad. 1: Management power is good. Bit [4] 0: Payload power is disabled. 1: Payload power is enabled. Bit [5] 0: Payload power is bad. 1: Payload power is good. Bit [6] 0: IPMB-L buffer is not attached. 1: IPMB-L buffer is attached. Bit [7] 0: IPMB-L buffer is not ready. 1: IPMB-L buffer is ready.

8.4.20 Enable Module Site Command

The Enable Module Site command is used to enable a module site.

Table 8-54 Enable Module Site Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
	4	Module Site ID
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00

8.4.21 Disable Module Site Command

The Disable Module Site command is used to disable a module site. If a module site is disabled, the IPMC firmware ignores the module inserted and acts as if the module is not present.

Table 8-55 Disable Module Site Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
	4	Module Site ID
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00

8.4.22 Reset Carrier SDR Repository Command

The Reset Carrier SDR Repository command is used to clear and rebuild the carrier SDR repository.

Table 8-56 Reset Carrier SDR Repository Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00

9.1 FRU Information

The blade provides the following FRU information in FRU ID 0.

Table 9-1 FRU Information

Area	Description	Value	Access
Internal use area	Not used		
Board info area	Mfg date / time	According to Platform Management FRU information Storage Definition v1.0	r
	Board manufacturer	'EMERSON'	r
	Board product name		r
	Board serial number		r
	Board part number		r
Product info area	Product manufacturer	'EMERSON'	r
	Product name	'ATCA-7370'	r
	Product part number	Defined by Artesyn Network Power - Embedded Computing	r
	Product serial number	Defined by Artesyn Network Power - Embedded Computing	r
Multi record info area	PICMG Blade Point-To-Point Connectivity Record Area	This multi record area contains the ATCA-blade Point to Point Connectivity Record according to PICMG 3.0, Rev.1.0.	r
	Carrier information Record	Defined by AMC.0 R2.0 Spec	r
	PICMG Carrier Activation and Current Management	Defined by AMC.0 R2.0 Spec	r
	PICMG Carrier Point-to-Point Connectivity Record	Defined by AMC.0 R2.0 Spec	r
	PICMG AMC Point-to-Point Connectivity	Defined by AMC.0 R2.0 Spec	r

Table 9-1 FRU Information (continued)

Area	Description	Value	Access
	OEM MAC Address Record		r

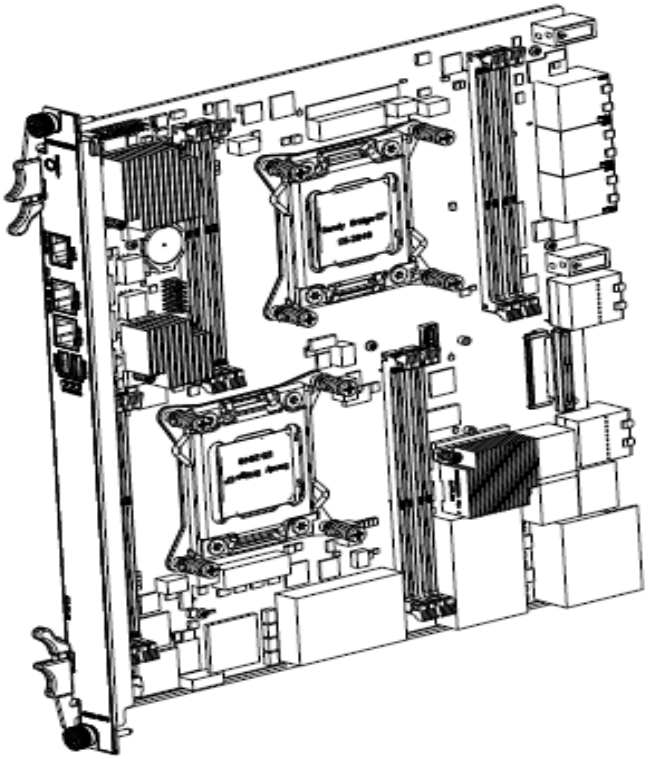
9.2 Power Configuration

Table 9-2 Power Configuration

Item	Value	Description
Dynamic power reconfiguration support	No	While the blade is powered, it supports only one power level.
Dynamic power configuration	No	The power level is fixed and does not change).
Number of power draw levels	3	The amount of possible power levels
Early Power Draw Levels, Watt	-	Complete early power level including IPMC
Steady state Power Draw Levels, Watt	1 = 120W 2 = 170W 3=200W	Complete steady power consumption including IPMC
Transition from early to steady levels, sec	0s	-

The following figure shows the locations of all temperature sensors available on-board.

Figure 9-1 Block Diagram



Note: On the single processor variant the processor and its DIMM sockets are populated on the upper side of the board. Components associated with the second processor are not populated on this product variant.

9.3 Sensor Data Records

The sensors available on the blades are detailed in the table below.

For sensor threshold definition please use the "ipmitool" found on http://sourceforge.net/projects/ipmitool/files/ipmitool/ with the parameter "sensor".

Table 9-3 Sensor Data Records

Sensor Number	Sensor Name	Sensor Type	Event/Reading Type	Event Data Byte 1	Event Data Byte 2	Event Data Byte 3	Event Threshold/ Description	Assertion Deassertion	Rearm
0	HS Carrier	Hot Swap 0xF0	Sensor-specific discrete 0x6F	0x0 0x1 0x2 0x3 0x4 0x5 0x6 0x7	[7:4] = Cause [3:0] = Previous State	FRU ID	0x0: M0 0x1: M1 0x2: M2 0x3: M3 0x4: M4 0x5: M5 0x6: M6 0x7: M7	Asrt	Auto
1	Hot Swap RTM	Hot Swap 0xF0	Sensor-specific discrete 0x6F	0x0 0x1 0x2 0x3 0x4 0x5 0x6 0x7	[7:4] = Cause [3:0] = Previous State	FRU ID	0x0: M0 0x1: M1 0x2: M2 0x3: M3 0x4: M4 0x5: M5 0x6: M6 0x7: M7	Asrt	Auto
2	-48V A Volts	Voltage 0x02	Threshold 0x01		reading	threshold	unr uc lnr lc	Asrt / Deass	Auto
3	-48V B Volts	Voltage 0x02	Threshold 0x01		reading	threshold	unr uc lnr lc	Asrt / Deass	Auto

Table 9-3 Sensor Data Records (continued)

Sensor Number	Sensor Name	Sensor Type	Event/Reading Type	Event Data Byte 1	Event Data Byte 2	Event Data Byte 3	Event Threshold/ Description	Assertion Deassertion	Rearm
4	-48V Current	Current 0x03	Threshold 0x01		reading	threshold	unr uc unc	Asrt / Deass	Auto
5	HoldUp Volts	Voltage 0x02	Threshold 0x01		reading	threshold	unr uc lnr lc	Asrt / Deass	Auto
6	Input Power	Other Units-based Sensor 0x0B	Threshold 0x01		reading	threshold	unr uc unc	Asrt / Deass	Auto

Table 9-3 Sensor Data Records (continued)

Sensor Number	Sensor Name	Sensor Type	Event/Reading Type	Event Data Byte 1	Event Data Byte 2	Event Data Byte 3	Event Threshold/ Description	Assertion Deassertion	Rearm
7	PWR Status	OEM 0xD7	Sensor-specific discrete 0x6F	0x0	Synchor Pwr Entr Module: [6] = VOUT_low [5] = Hotswap [4] = Holdup [2] = Alarm [1] = Enable_B [0] Enable_A Emerson Pwr Entry Module: [7] = DIG_Fault [6] = HUCapEngage [5] = Hotswap_Enable [4] = HUCap_Switch [3] = Alarm_Control [1] = DIG_Alarm [0] = Sec_MCU_Fault All other bits are reserved	[7:6] = Pwr Entry Module 0 = Synchor 1 = Emerson Emerson Pwr Entry Module: [2] = DIG_EnableA [1] = DIG_EnableB [0] = Mcu_Fault All other bits are reserved	0x0: Pwr Entry Module Status Change detected	Asrt	Auto
8	Inlet Temp	Temp 0x01	Threshold 0x01		reading	threshold	unr uc unc	Asrt / Deass	Auto
9	Outlet Temp	Temp 0x01	Threshold 0x01		reading	threshold	unr uc unc	Asrt / Deass	Auto
10	Board Temp	Temp 0x01	Threshold 0x01		reading	threshold	unr uc unc	Asrt / Deass	Auto

Table 9-3 Sensor Data Records (continued)

Sensor Number	Sensor Name	Sensor Type	Event/Reading Type	Event Data Byte 1	Event Data Byte 2	Event Data Byte 3	Event Threshold/ Description	Assertion Deassertion	Rearm
11	CPU0 VR Temp	Temp 0x01	Threshold 0x01		reading	threshold	unr uc unc	Asrt / Deass	Auto
12	DDR VR0 Temp	Temp 0x01	Threshold 0x01		reading	threshold	unr uc unc	Asrt / Deass	Auto
13	DDR VR1 Temp	Temp 0x01	Threshold 0x01		reading	threshold	unr uc unc	Asrt / Deass	Auto
14	CPU0 Temp	Temp 0x01	Threshold 0x01		reading	threshold	unr uc unc	Asrt / Deass	Auto
15	DDR 1 Temp	Temp 0x01	Threshold 0x01		reading	threshold	unr uc unc	Asrt / Deass	Auto
16	DDR 2 Temp	Temp 0x01	Threshold 0x01		reading	threshold	unr uc unc	Asrt / Deass	Auto
17	DDR 3 Temp	Temp 0x01	Threshold 0x01		reading	threshold	unr uc unc	Asrt / Deass	Auto
18	DDR 4 Temp	Temp 0x01	Threshold 0x01		reading	threshold	unr uc unc	Asrt / Deass	Auto
19	12.0V	Temp 0x01	Threshold 0x01		reading	threshold	unr uc lnr lc	Asrt / Deass	Auto
20	3.3V	Temp 0x01	Threshold 0x01		reading	threshold	unr uc lnr lc	Asrt / Deass	Auto
21	1.1V PCH	Voltage 0x02	Threshold 0x01		reading	threshold	unr uc lnr lc	Asrt / Deass	Auto

Table 9-3 Sensor Data Records (continued)

Sensor Number	Sensor Name	Sensor Type	Event/Reading Type	Event Data Byte 1	Event Data Byte 2	Event Data Byte 3	Event Threshold/ Description	Assertion Deassertion	Rearm
22	1.8V CPU PLL	Voltage 0x02	Threshold 0x01		reading	threshold	unr uc lnr lc	Asrt / Deass	Auto
23	VTT CPU	Voltage 0x02	Threshold 0x01		reading	threshold	unr uc lnr lc	Asrt / Deass	Auto
24	VSA CPU	Voltage 0x02	Threshold 0x01		reading	threshold	unr uc lnr lc	Asrt / Deass	Auto
25	VCC CPU	Voltage 0x02	Threshold 0x01		reading	threshold	unr uc lnr lc	Asrt / Deass	Auto
26	1.5V DDR3	Voltage 0x02	Threshold 0x01		reading	threshold	unr uc lnr lc	Asrt / Deass	Auto
27	IPMB0 Link	Physical IPMB-0 0xF1	Sensor-specific discrete 0x6F	0x0 0x1 0x2 0x3	[7:4] = Channel Number [3:0] = Reserved	reading	0x0: IPMB-A disabled, IPMB-B disabled 0x1: IPMB-A enabled, IPMB-B disabled 0x2: IPMB-A disabled, IPMB-B enabled 0x3: IPMB-A enabled, IPMB-B enabled	Asrt / Deass	Auto

Table 9-3 Sensor Data Records (continued)

Sensor Number	Sensor Name	Sensor Type	Event/Reading Type	Event Data Byte 1	Event Data Byte 2	Event Data Byte 3	Event Threshold/ Description	Assertion Deassertion	Rearm
28	BMC Watchdog	Watchdog 2 0x23	Sensor-specific discrete 0x6F	0x0 0x1 0x2 0x3 0x4 0x8	See IPMI Spec	0xFF	0x0: Timer expired 0x1: Hard Reset 0x2: Power Down 0x3: Power Cycle 0x8: Timer Interrupt	Asrt	Auto
29	IPMC POST	Management Subsystem Health 0x28	digital Discrete 0x06	0x0 0x1	0xFF	0xFF	0x0: Performance Met 0x1: Performance Lags	Asrt	Auto

Table 9-3 Sensor Data Records (continued)

Sensor Number	Sensor Name	Sensor Type	Event/Reading Type	Event Data Byte 1	Event Data Byte 2	Event Data Byte 3	Event Threshold/ Description	Assertion Deassertion	Rearm
30	Ver Change	Version Change 0x2B	Sensor-specific discrete 0x6F	0x0 0x1 0x2 0x3 0x4 0x5 0x6 0x7	Change type	0xFF	0x0: Hardware change 0x1: Firmware or software change 0x2: Hardware incompatibility 0x3: Firmware or software incompatibility 0x4: Entity is of an invalid hardware version 0x5: Entity contains invalid F/W,software 0x6: Hardware Change successful 0x7: Software or F/W change successful.	Asrt	Auto
31	FW Progress	System Firmware Progress 0x0F	Sensor-specific discrete 0x6F	0x0 0x1 0x2	See IPMI Spec	See IPMI Spec	0x0: System Firmware Error 0x1: System Firmware Hang 0x2: System Firmware Progress	Asrt	Auto

Table 9-3 Sensor Data Records (continued)

Sensor Number	Sensor Name	Sensor Type	Event/Reading Type	Event Data Byte 1	Event Data Byte 2	Event Data Byte 3	Event Threshold/ Description	Assertion Deassertion	Rearm
32	OS Boot	OS Boot 0x1F	Sensor-specific discrete 0x6F	0x0 0x1 0x2 0x3 0x4 0x5 0x6	0xFF	0xFF	0x0: A: boot completed 0x1: C: boot completed 0x2: PXE boot completed 0x3: Diagnostic boot completed 0x4: CD_ROM boot completed 0x5: ROM boot completed 0x6: boot completed	Asrt	Auto
33	Boot Error	Boot Error 0x1E	Sensor-specific discrete 0x6F	0x0 0x1 0x2 0x3 0x4	0xFF	0xFF	0x0: No Bootable media 0x1: Non-bootable diskette 0x2: PXE Server not found 0x3: Invalid boot sector 0x4: Timout waiting for user selection	Asrt	Auto

Table 9-3 Sensor Data Records (continued)

Sensor Number	Sensor Name	Sensor Type	Event/Reading Type	Event Data Byte 1	Event Data Byte 2	Event Data Byte 3	Event Threshold/ Description	Assertion Deassertion	Rearm
34	Boot Inited	System Boot Initiated 0x1D	Sensor-specific discrete 0x6F	0x0 0x1 0x2 0x3 0x4	0xFF	0xFF	0x0: Initiated by power up 0x1: Initiated by hard reset 0x2: Initiated by warm reset 0x3: User requested PXE boot 0x4: Automatic boot to diagnostic	Asrt	Auto
35	POST Code	OEM 0xD1	Sensor-specific discrete 0x6F	0x0 0x1 0x2 0x3 0x4 0x5 0x6 0x7	0xFF	Reading according to EFI BIOS port80 status codes	0x0: BIOS POST Code 0x3: 209 0x4: OEM 0xD1 0x6: 0xFF 0x7: Reading according to EFI BIOS port80 status codes.	Asrt	Auto

Table 9-3 Sensor Data Records (continued)

Sensor Number	Sensor Name	Sensor Type	Event/Reading Type	Event Data Byte 1	Event Data Byte 2	Event Data Byte 3	Event Threshold/ Description	Assertion Deassertion	Rearm
36	IPMC Status	OEM 0xD5	Sensor-specific discrete 0x6F	0x0 0x1 0x2 0x3 0x4 0x5 0x6	-	-	0x0: Watchdog Reset 0x1: Software Reset 0x2: Power Failure 0x3: Hard Boot 0x4: Cold Boot 0x5: Warm Boot 0x6: Reserved		Auto
37	Power Good	Power Supply 0x08	Sensor-specific discrete 0x6F	0x0 0x1	See IPMI Spec	0xFF	0x0: Presence detected 0x1: Power Supply Failure detected	Asrt	Auto
38	Boot Bank	OEM 0xD2	Sensor-specific discrete 0x6F	0x0	0xFF	0xFF	0x0: Boot Bank A	Asrt	Auto

Table 9-3 Sensor Data Records (continued)

Sensor Number	Sensor Name	Sensor Type	Event/Reading Type	Event Data Byte 1	Event Data Byte 2	Event Data Byte 3	Event Threshold/ Description	Assertion Deassertion	Rearm
39	Reset Source	OEM 0xDA	Sensor-specific discrete 0x6F	0x0 0x1 0x2 0x3 0x4 0x5 0x6 0x7 0x8 0x9 0xA 0xB 0xC 0xD 0xE	[7] = OS reset payload req. [6] = BIOS reset payload req. [5] = FPGA Watchdog Reset [4] = Push Button Reset RTM [3] = IPMC reset payload req. [2] = Pus Button Reset front [1] = reserved [0] = Payload Power-on reset	[7:2] = Reserved [1] = IPMC Pre-Timout [0] = IPMC Watchdog Timeout	0x0: Payload Reset detected. Cause delivered in Event Byte 2/3	Asrt	Auto
40	CPU Status	Processor 0x07	Sensor-specific discrete 0x6F	0x1 0xA	0xFF	0xFF	0x1: Thermal Trip 0xA: ProcHot	Asrt	Auto
41	ACPI State	System ACPI Power State 0x22	Sensor-specific discrete 0x6F	0x0 0x3 0x5	0xFF	0xFF	0x0: S0 0x3: S3 0x5: S5	Asrt	Auto

Firmware Upgrade

10.1 HPM.1 Firmware Upgrade

10.1.1 Overview

The primary update mechanism for the ATCA-7370 blades is the FCU tool which is delivered with the BBS package for the board. However, the ATCA-7370 board family also supports upgrade of the firmware with the HPM.1 specification. Upgradable components of the board include the BIOS flash, FPGA flash, and IPMC flash. For update, it is recommended to use the Pigeon Point System modified Ipmitool.

10.1.2 Installing the ipmitool

Refer *Installing the ipmitool* on page 175, for installing the ipmitool procedure.

10.1.2.1 Update Procedure

The Ipmitool HPM update requires two steps for an update:

1. Upgrade the component.
   Example: **`ipmitool hpm upgrade <file>`**
2. Activate the component.
   Example: **`ipmitool hpm activate`**

Both steps can also be integrated into one command.

```
ipmitool hpm upgrade <file> activate
```

10.1.3 Interface

The HPM.1 upgrade supports three different interfaces for upgrading the firmware. These are KCS, IPMB-0, and LAN over BASE. The LAN interface is only supported when the payload is powered on (M4). The BASE Ethernet controller also has to be powered on for this feature.

10.1.3.1 KCS Interface

The standard way to upgrade the firmware of the payload is through the KCS interface. Upgrade through this interface is the fastest HPM.1 upgrade. The images and the ipmitool need to be on the payload to be upgraded.

Example:

```
Prompt>ipmitool hpm upgrade <file>
```

10.1.3.2 IPMB-0

This interface represents the backplane IPMI bus and allows remote firmware upgrade. The count of the simultaneous upgrades is limited because of the bus speed.

Example from shelf manger:

```
Prompt>ipmitool -t 0x92 hpm upgrade <file>
```

Example with RMCP:

```
Prompt>ipmitool -I lan -H 192.168.34.8 -U Administrator -P
Administrator -t 0x92 hpm upgrade <file>
```

10.1.3.3 IPMI Over LAN (BASE)

The IPMI over LAN interface uses the BASE Ethernet controller to do firmware upgrades. The interface has to be configured before the first use. Configuring this interface is described in Chapter 7, *Configuring SOL Parameters*, on page 176.

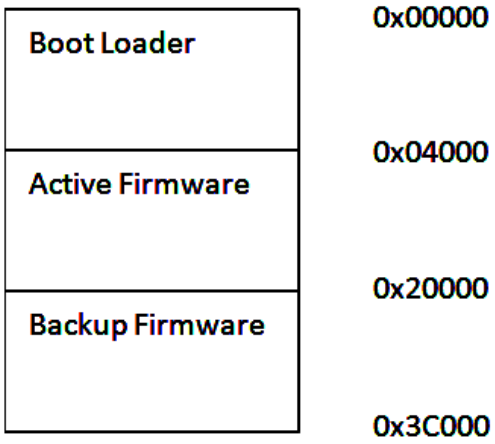
Example:

```
Prompt>Ipmitool -I lan -H 172.16.0.221 -U "" -P "" hpm upgrade
<file>
```

10.2 IPMC Upgrade

The IPMC component is fully HPM.1 compatible and contains three elements as shown in the figure below.

Figure 10-1 IPMC Component Elements



There are images for the boot loader and the firmware. There is also a combined image containing the boot loader and the firmware. The Boot loader update should only be done if it's required.

The boot loader does not perform any upgrade action. The boot loader is able to boot either of two redundant copies of the firmware in the flash depending on the current value of the special partition status byte that is stored in the internal IPMC EEPROM. The boot loader can fall back to the backup copy by booting the alternate partition.

The boot loader manages both; active and backup firmware partitions. It is responsible for detecting if the active firmware is invalid or has failed. In either case, the Boot loader will switch to the backup partition. After switching, the partitions change their roles. Switching of the partitions also takes place when the firmware is upgraded and activated using the HPM.1 upgrade procedure.

The firmware image is the regular firmware and change with every update.

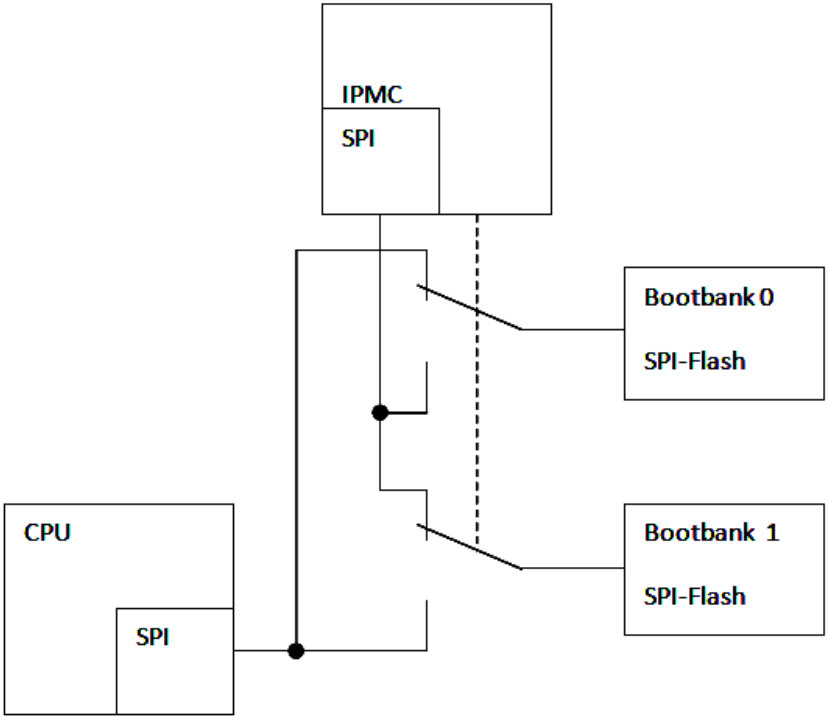
10.3 BIOS/FPGA Update

Both BIOS and FPGA components have two independent boot banks.

Both BIOS and FPGA boot banks can be upgraded with HPM.1. IPMC support automatic boot bank switching, which is mandaory for HPM.1 to activate. The newly upgrade firmware can be activated with a payload power cycle if you upgraded the firmware with activate option.

Payload always has access to the active boot bank and the IPMC always has access to the inactive boot bank. All HPM.1 commands are directed to the inactive boot bank (this includes "get component properties"). The following figure shows the connection of the SPI busses which are switched with "Set System Boot Options" -> Boot Bank (parameter 0x96). Description can be found in the *System Boot Options Parameter #96* on page 186.

Figure 10-2 SPI Busses Connection



FPGA and BIOS upgrade may last from fifteen minutes up to two hours. The time varies with the selected programming interface. A power cycle is required after the BIOS/FPGA update.

10.4 Upgrade Package

The HPM upgrade package for this release contains the following files:

Table 10-1 HPM Upgrade Package

Filename	Description
atca7370_em_bios_xx_yy_zzzz.hpm	Contains BIOS HPM.1 image with version xx_yy_zzzz
atca7370_em_fpga_xx_yy_zzzz.hpm	Contains FPGA HPM.1 image with version xx_yy_zzzz
atca7370_em_ibbl_ xx_yy_zzzz.hpm	Contains IPMC boot loader image with version xx_yy_zzzz
atca7370_em_ipmc_ xx_yy_zzzz.hpm	Contains IPMC firmware with version xx_yy_zzzz

A.1 Error List

This chapter can be taken as an error list for detecting erroneous configurations and strange behaviors. It cannot replace a serious and sophisticated pre- and post-sales support during application development.

If it is not possible to fix a problem with the help of this chapter, contact your local sales representative or Field Application Engineer (FAE) for further support.

A.1.1 CPU Blade is Not Functioning Properly

The following table lists the errors, reasons and solutions for which the CPU blade is not functioning properly.

Errors	Possible Reasons	Solution
• The power good LED is not lit • The out-of-service LED is lit • The hot swap LED is not lit when the hot swap latch is opened, or lits when the latch is closed • The console redirection does not display BIOS POST • The BIOS output does not include the expected data • The blade does not answer to ping • There is an IPMI alarm	The embedded software in the hardware units is not consistent with the product release.	Verify the software is consistent with the product release.
	The blade is not properly seated.	Make sure that the blade is properly seated.
	One of the memory modules is not properly seated.	Make sure that the memory module is properly seated.
	One of the cables is not properly connected	Connect the cable properly.
	The FRU data of the blade is incorrect.	Verify the FRU data of the blade.
	One of the voltages is too high or low.	Make sure the voltage is as per the board requirements.
	One of the temperatures is too high.	Make sure the temperature is as per the board requirements.
	There is a fault in the DC converter.	Verify the DC converter.
	The IP address of the blade is incorrect.	Verify the IP address of the blade.

Related Documentation

B.1 Artesyn Embedded Technologies - Embedded Computing Documentation

The publications listed below are referenced in this manual. You can obtain electronic copies of Artesyn Embedded Technologies - Embedded Computing publications by contacting your local Artesyn sales office. For released products, you can also visit our Web site for the latest copies of our product documentation.

1. Go to www.artesyn.com/computing/support/product/technical-documentation.php.
2. Under FILTER OPTIONS, click the Document types drop-down list box to select the type of document you are looking for.
3. In the Search text box, type the product name and click GO.

Table B-1 Artesyn Embedded Technologies - Embedded Computing Publications

Document Title	Publication Number
ATCA-7370/ATCA-7370-S Quick Start Guide	6806800P66
ATCA-7370/ATCA-7370-S Safety Notes Summary	6806800P67

B.2 Related Specifications

For additional information, refer to the following table for related specifications. As an additional help, a source for the listed document is provided. Please note that, while these sources have been verified, the information is subject to change without notice.

Table B-2 Related Specifications

Organization	Document Title
PCI-SIG	PCI Local Bus Specification Revision 2.2 PCI-X Addendum to the PCI Local Bus Specification 1.0
PICMG	PICMG 3.0 Revision 2.0 Advanced TCA Base Specification PICMG 3.1 Revision 1.0 Specification Ethernet/Fiber Channel for AdvancedTCA Systems

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